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ILI6480B

Single Chip for 480RGBx272 TFT Panel 720x544 Driver with Timing Controller

Specification
Preliminary

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Table of Contents

Section ***Page***

1. Introduction

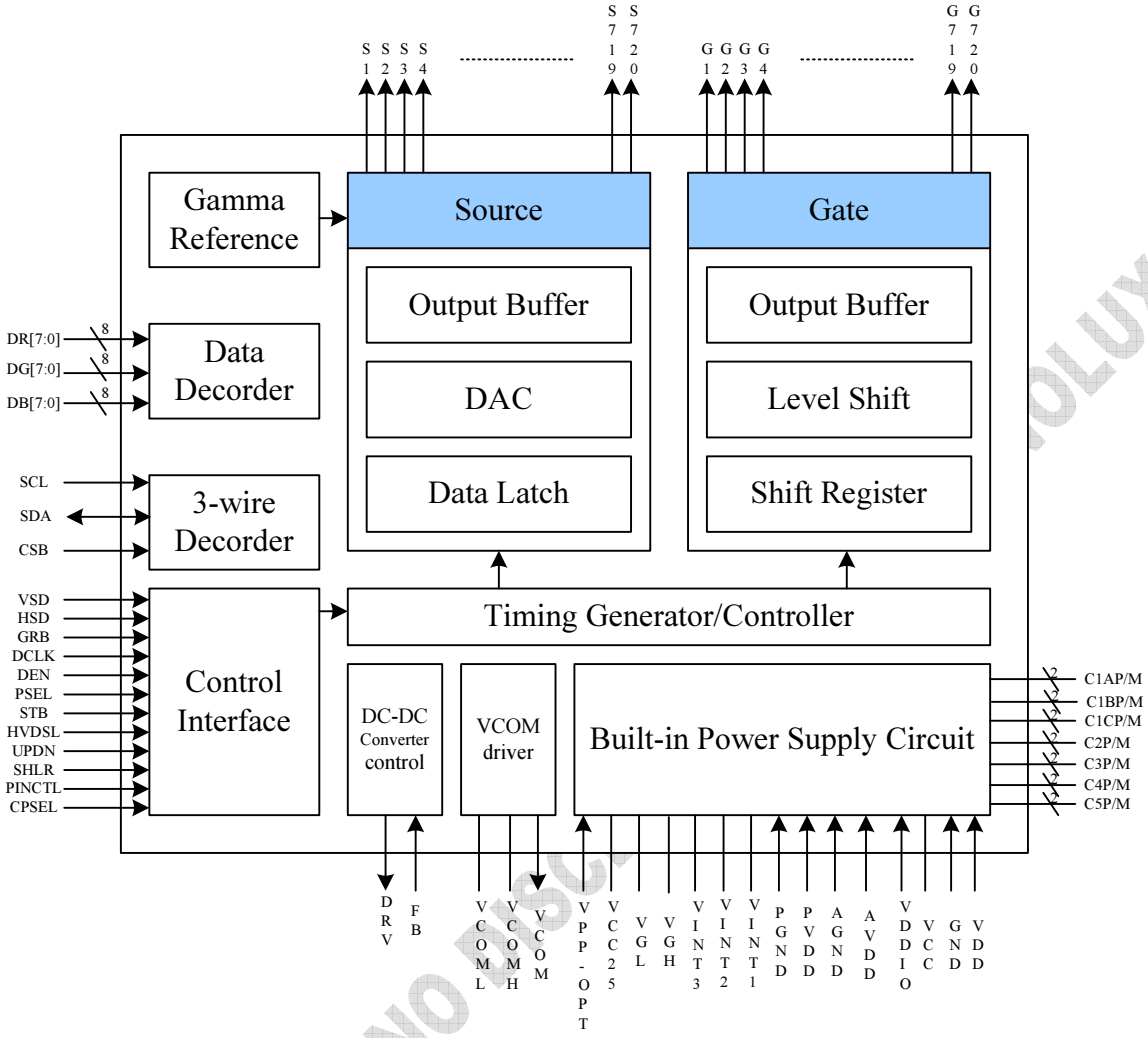
ILI6480B is one-chip solution for a-TFT LCD panel. The panel application is focused on the resolution of 480RGBx272. The source driver, gate driver, built-in power generator and timing controller are integrated in the ILI6480B. The serial communication interface is also implemented for the register setting. This chip can operates in a wide range of supply voltage.

By applying “Dual Gate Driver” panel architecture, the number of source output is reduced to 720 channels and the number of gate output is increased to 544 channels. For the concern of lower power dissipation, line inversion driving technique was adopted. With dithering technique applied, source output support 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution.

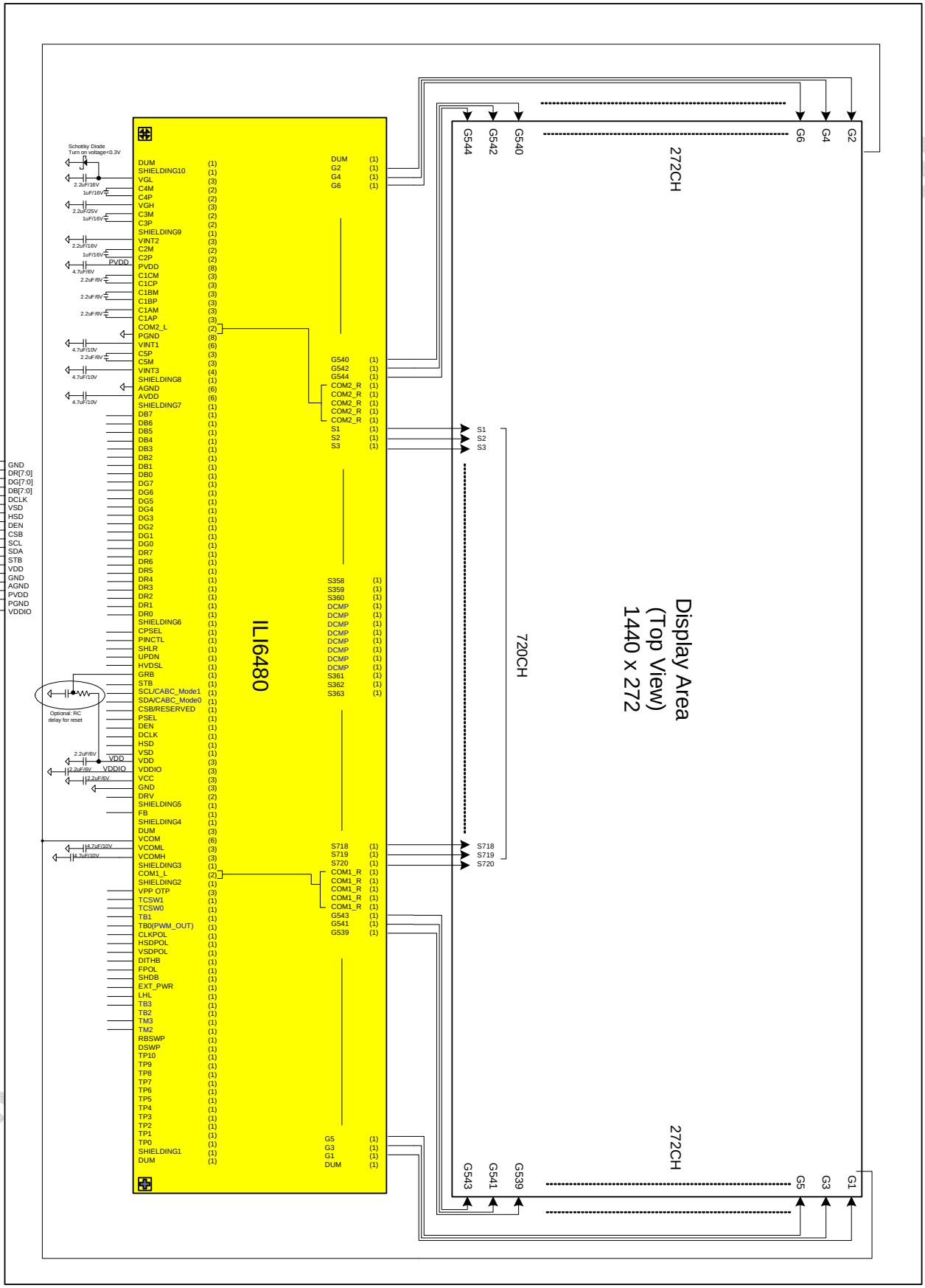
2. Features

- Generate 720x544 TFT control signals with timing controller
- Panel resolution(HxV): 480[RGB]x272
- 8-bit resolution 256 gray scale with Dithering(7bits DAC + 1 bit FRC)
- Display control and function select by 3-wire serial communication control.
- Build-in DC/DC charge pump, regulator and VCOM with programmable adjustment
- Source output deviation: ±20mV
- Line inversion or half-line inversion selectable
- Right/Left shift, Up and Down scan function selectable
- Build-In PWM circuit for LED backlight
- Power for digital circuit(VDD): 3.0V~ 3.6V
- Power for analog circuit(PVDD): 3.0V ~ 3.6V
- Power for interface (VDDIO): 1.8V ~ 3.6V

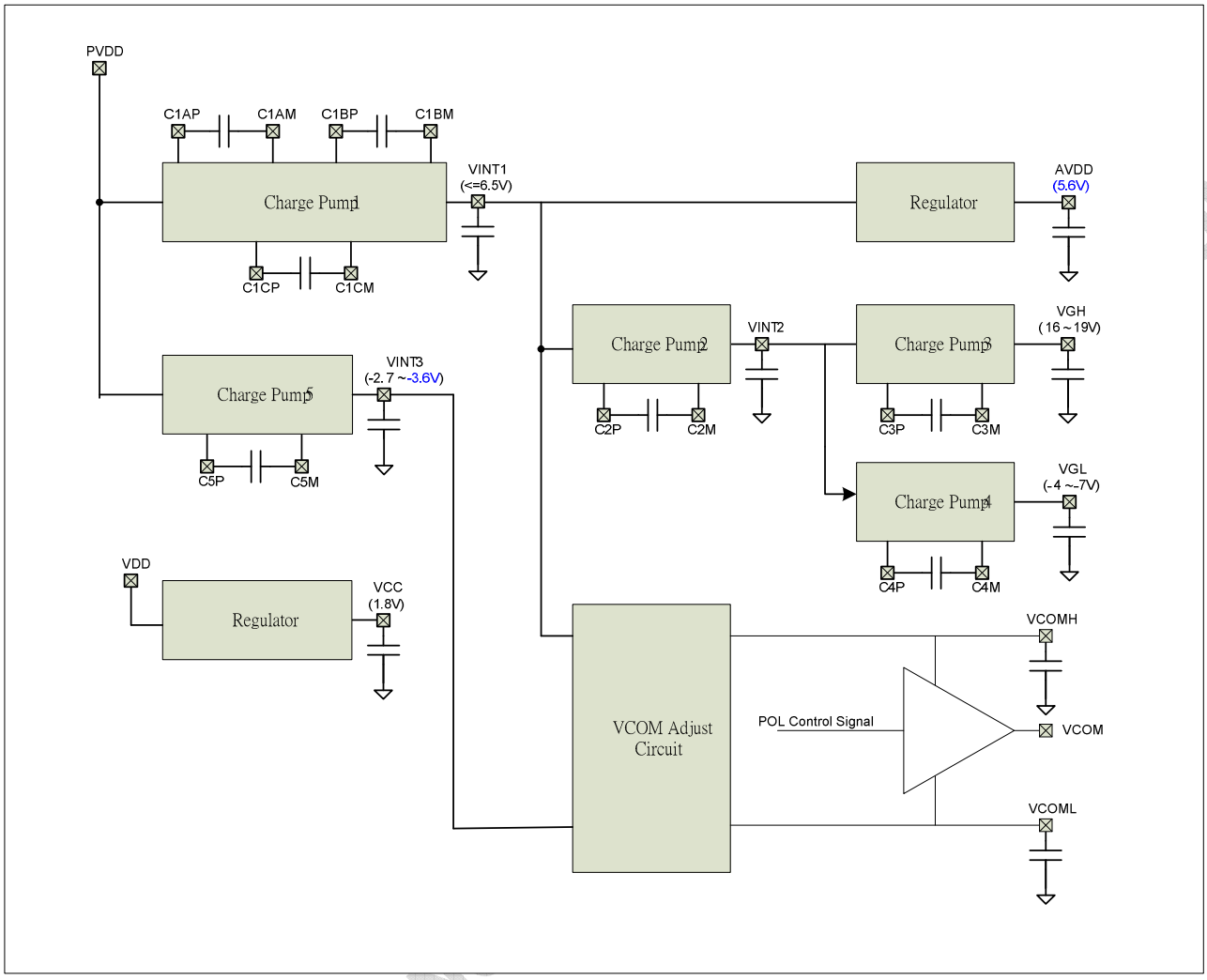
3. Block Diagram



4. Application Block



5. Charge Pump Circuit Block



6. Pin Descriptions

Pin Name	I/O	Descriptions
HSD	I (VDDIO)	Horizontal Sync input. Negative polarity. ***Remark: Internal pulled weak high**
VSD	I (VDDIO)	Vertical Sync input. Negative polarity. ***Remark: Internal pulled weak high**
DCLK	I (VDDIO)	Clock signal. Latching data at the rising edge
DEN	I (VDDIO)	Data input Enable. Active High to enable the data input Bus under “DE Mode”. ***Remark: Internal pulled weak low**
PSEL	I (VDDIO)	Parallel 24-bit and Serial 8-bit data input selection. PSEL=”H”, Parallel 24-bit RGB input through DR[7:0], DG[7:0], DB[7:0], PSEL=”L”, Serial 8-bit data input through DR[7:0] ***Remark: Internal pulled weak high**
DR[7:0]	I (VDDIO)	When PSEL=”H”, these will be treated as Parallel 8-bit digital Red data input. When PSEL=”L”, these will be treated as serial 8-bit data input. ***Remark: Internal pulled weak low**
DG[7:0]	I (VDDIO)	8-bit digital Green data input, only valid when PSEL=”H” (Parallel mode). ***Remark: Internal pulled weak low**
DB[7:0]	I (VDDIO)	8-bit digital Blue data input, only valid when PSEL=”H” (Parallel mode). ***Remark: Internal pulled weak low**
CSB	I (VDDIO)	Multi function control pin. When TB1=”L”, this pin act as 3-wire “CSB” pin When TB1=”H”, reserved. *** Remark: Internal pulled weak high**
SDA	I/O (VDDIO)	Multi function control pin. When TB1=”L”, this pin act as 3-wire “SDA” pin. When TB1=”H”, this pin act as CABC mode select pin LSB (CABCM[0]) *** Remark: Internal pulled weak low**
SCL	I (VDDIO)	Multi function control pin. When TB1=”L”, this pin act as 3-wire “SCL” pin. When TB1=”H”, this pin act as CABC mode select pin MSB (CABCM[1]) CABCM[1:0] = 00b, OFF (default) CABCM[1:0] = 01b, User interface image CABCM[1:0] = 10b, Still picture CABCM[1:0] = 11b, Moving image ***Remark: Internal pulled weak low**
STB	I (VDDIO)	Standby setting for testing, it should be connected to VDDIO in normal operation mode. If connected to GND, the IC is in standby mode. ***Remark: Internal pulled weak high**
GRB	I (VDDIO)	Global reset pin, it should be connected to VDDIO in normal operating mode. If connected to GND, the timing controller is in reset state, suggest to be connected with a RC reset circuit for stability. ***Remark: Internal pulled weak high**
HVDSL	I (VDDIO)	HV mode or DE mode control signal. HVDSL=”H”: Set under HV mode, VSD and HSD signal have to provide by system. HVDSL=”L”: Set under DE mode, DE signal have to provide by system. ***Remark: Internal pulled weak low**
UPDN	I (VDDIO)	Gate driver Up/Down scan control of gate driver. UPDN=”H”, Shift from up to down, First line=L1->L2-> … ->L543->L544=Last line UPDN=”L”, Shift from down to up, First line=L544->L543-> … ->L2->L1=Last line ***Remark: Internal pulled weak high**
SHLR	I (VDDIO)	Right/Left sequence control of source driver. SHLR=”H”, Shift right: First data=S1->S2->S3 … ->S720=Last data SHLR=”L”, Shift left: Last data=S1<-S2<-S3 … <-S720=First data ***Remark: Internal pulled weak high**

Pin Name	I/O	Descriptions
TB0 (PWM_OUT)	O (VDDIO)	PWM output control signal for CABC function
TB1	I (VDDIO)	CABC/3-wire selection pin TB1="H", Select CABC hardware control function. TB1="L", Select 3-wire SPI interface function. ***Remark: Internal pulled weak low**
PINCTL	I (VDDIO)	Enable pin control function PINCTL="H", Enable pin control function PINCTL="L", Disable pin control function ***Remark: Internal pulled weak low** **Note: The 3-wire related control register will be disabled under PINCTL="H"**
CPSEL	I (VDDIO)	Charge pump structure select pin. CPSEL="H", C1CP/M is connected to capacitor.. CPSEL="L", C1CP/M is floating ***Remark: Internal pulled weak low**
EXT_PWR	I (VDDIO)	External power control pin. EXT_PWR="H": VINT1 could be input externally. EXT_PWR="L": VINT1 is generated by charge pump circuit. ***Remark: Internal pulled weak low**
VSDPOL	I (VDDIO)	VSD polarity control pin. VSDPOL="H": VSD positive polarity. VSDPOL="L": VSD negative polarity. ***Remark: Internal pulled weak low**
HSDPOL	I (VDDIO)	HSD polarity control pin. VSDPOL="H": HSD positive polarity. VSDPOL="L": HSD negative polarity. ***Remark: Internal pulled weak low**
CLKPOL	I (VDDIO)	DCLK polarity control pin. CLKPOL="H": Data sampling at DCLK falling edge. CLKPOL="L": Data sampling at DCLK rising edge. ***Remark: Internal pulled weak low**
FPOL	I (VDDIO)	VCOM polarity inverse control pin. When FPOL="H", VCOM inverse polarity. When FPOL="L", VCOM normal polarity. ***Remark: Internal pulled weak low**
DITHB	I (VDDIO)	Dithering control pin. DITHB="H", Dithering off, (7-bits resolution, truncation last 1-bits of the input data) DITHB="L", Dithering on, (Pseudo 8-bits resolution). ***Remark: Internal pulled weak low**
SHDB	I (VDDIO)	Shut down for back light power converter. SHDB="H", The back light power converter is controlled by STB's power on/off sequence SHDB="L", The back light power converter is off. ***Remark: Internal pulled weak low**
LHL	I (VDDIO)	Line/Half-Line inversion control pin. LHL="H", Half line inversion. (Default) LHL="L", Line inversion. ***Remark: Internal pulled weak high**
FB	I	Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6V nominal.
DRV	O	Power transistor gate signal for the boost converter.
VDD	P	Power supply for digital circuits
GND	P	Ground for digital circuits.
PVDD	P	Power supply for analog circuits.
PGND	P	Ground pin for power circuits.
AGND	P	Ground pin for analog circuits.
VDDIO	P	Power supply for logic I/O.
VPP_OTP	P	Customer OTP power input pin.

Pin Name	I/O	Descriptions
VCC	C	Capacitor connect pin for internal regulator.
AVDD	C	Power setting capacitor connect pin.
VINT1	C	Power setting capacitor connect pin.
VINT2	C	Power setting capacitor connect pin.
VINT3	C	Power setting capacitor connect pin.
VGH	C	Power setting capacitor connect pin.
VGL	C	Power setting capacitor connect pin.
C1AP/M C1BP/M C1CP/M C2P/M C3P/M C4P/M C5P/M	C	Capacitor connect pin for internal charge pump. Refer to the section of “Power Circuit” for the application.
VCOM	O	Panel COMMON plate output.
VCOMH	C	Power supply for panel COMMON plate high level output.
VCOML	C	Power supply for panel COMMON plate low level output.
S720 ~ 1	O	Source driver output signals.
G544 ~ 1		Gate driver output signals.
DCMP	O	Test Pin. Please let this pin open.
ALIGN_R ALIGN_L	M	For assembly alignment.
COM1_L COM1_R	S	The internal link together between input side and output side.
COM2_L COM2_R	S	The internal link together between input side and output side.
DSWP	I	Data sequence control pin. When DSWP=”H”, swap data sequence. When DSWP =”L”, normal data sequence. ***Remark: Internal pulled weak low**
RBSWP	I	R/B swap control pin. When RBSWP =”H”, R→B, B→R When RBSWP =”L”, normal data. ***Remark: Internal pulled weak low**
TP[10:0]	T	Test pins for internal testing only. ***Remark: Not connected.**
TCSW0	I (VDDIO)	Enable pin control funciotn. TCSW0=0 : VCOM frequency is fixed. TCSW0=1 : Split the VCOM frequency. ***Remark : Internal pulled weak low**
TCSW1	I (VDDIO)	Test pins for internal testing only. ***Remark : Internal pulled weak high**
TB2	T	Gate Scan select function. TB2=”H”, Scan method 1. TB2=”L”, Scan method 2. (Default) ***Remark: Internal pulled weak low**
TB3	T	Test pins for internal testing only. Leave this pin to be open. ***Remark : not connection.**
TM2	T	Test pins for internal testing only. Leave this pin to be open. ***Remark : not connection.**
TM3	T	Test pins for internal testing only. Leave this pin to be open. ***Remark : not connection.**
SHIELDING	S	This pin is internal floating. ***Remark: Not connected.**
DUM	D	Dummy pads. Leave this pin to be open.

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing
I/ O: Input / Output. PS: Power Setting, C: Capacitor pin.

Pass Line Description:

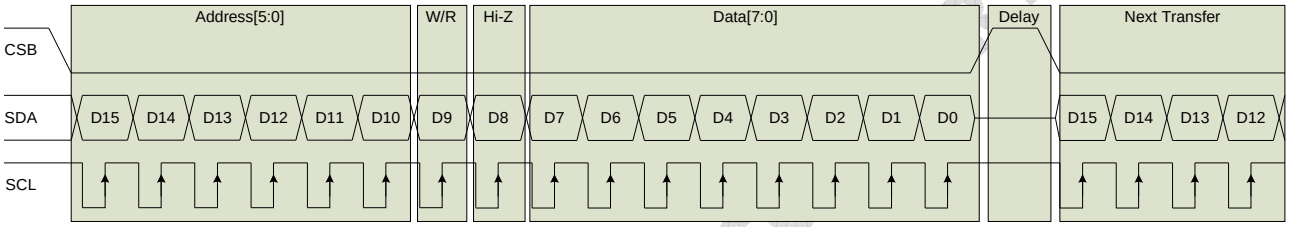
Pass Line no.	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

7. 3-wire Serial Interface

ILI6480B uses the 3-wire serial interface to set all the function and register parameter. The 3-wire serial interface is bi-directional and controlled by the R/W bit.

In the read mode, 3-wire serial interface will return the read data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored. During read operation, external controller should float SDA pin under the “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit to prevent from incorrect setting of the internal register; any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-wire serial interface.



Bit	Description
D[15:10]	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D[7:0]	Data for the W/R operation to the address indicated by Address phase

Note: Setting of all the registers will take effect at the coming falling edge of VSD signal except RESETB and STBYB bit.

8. Register List

N0	Address						R/W	D8	Parameter Data							
	D15	D14	D13	D12	D11	D10	D9		D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	R/W	x	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	FRAD1	FRAD0	DITHB
							1/0		0	0	0	0	0	0	0	0
R1	0	0	0	0	0	1	R/W	x	CABC_ MODE1	CABC_ MODE0	x	LHL	STB	GRB	SHRL	UPDN
							1/0		0	0	x	1	1	1	1	1
R2	0	0	0	0	1	0	R/W	x	X	VFBSEL		DRV_FREQ	PWM_DUTY[2:0]			SHDB
							1/0		X	0	1	0	0	1	1	0
R3	0	0	0	0	1	1	R/W	x	LED_ON_CYCLE[3:0]				LED_ON_RATIO[3:0]			
							1/0		0	1	1	1	1	1	1	1
R4	0	0	0	1	0	0	R/W	x	DDL[7:0]							
							1/0		0	0	1	0	1	0	0	0
R5	0	0	0	1	0	1	R/W	x	X	X	X	HDL[4:0]				
							1/0		X	X	X	0	1	0	0	0
R6	0	0	0	1	1	0	R/W	x	VCOMH_OTP	VCOMH [6]	VCOMH [5]	VCOMH [4]	VCOMH [3]	VCOMH [2]	VCOMH [1]	VCOMH [0]
							1/0		0	1	0	1	0	0	1	1
R7	0	0	0	1	1	1	R/W	x	VCOML_OTP	VCOML [6]	VCOML [5]	VCOML [4]	VCOML [3]	VCOML [2]	VCOML [1]	VCOML [0]
							1/0		0	0	1	1	1	1	1	0
R8	0	0	1	0	0	0	R/W	x	BRI[7:0]							
							1/0		0	1	0	0	0	0	0	0
R9	0	0	1	0	0	1	R/W	x	CON_B[7:0]							
							1/0		0	1	0	0	0	0	0	0
R10	0	0	1	0	1	0	R/W	x	X	SUB_BRI_R[6:0]						
							1/0		X	1	0	0	0	0	0	0
R11	0	0	1	0	1	1	R/W	x	X	SUB_CON_R[6:0]						
							1/0		X	1	0	0	0	0	0	0
R12	0	0	1	1	0	0	R/W	x	X	SUB_BRI_B[6:0]						
							1/0		X	1	0	0	0	0	0	0
R13	0	0	1	1	0	1	R/W	x	X	SUB_CON_B[6:0]						
							1/0		X	1	0	0	0	0	0	0
R14	0	0	1	1	1	0	R/W	x	CABC_ BRI1	CABC_ BRI0	V2GAM[3:0]				GAMEN	x
							1/0		0	1	1	0	0	0	1	x
R15	0	0	1	1	1	1	R/W	x	V4GAM[3:0]				V3GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R16	0	1	0	0	0	0	R/W	x	V6GAM[3:0]				V5GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R17	0	1	0	0	0	1	R/W	x	V8GAM[3:0]				V7GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R18	0	1	0	0	1	0	R/W	x	x	x	x	x	V9GAM[3:0]			
							1/0		x	x	x	x	1	0	0	0
R19	0	1	0	0	1	1	R/W	x	x	x	x	x	VGL_SEL[1:0]		VGH_SEL[1:0]	
							1/0		x	x	x	x	1	1	1	1
R20	0	1	0	1	0	0	R/W	x	TRMEN[7:0]							
							1/0		0	0	0	0	0	0	0	0
R21	0	1	0	1	0	1	R/W	x	V13GAM[3:0]				V12GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R22	0	1	0	1	1	0	R/W	x	V15GAM[3:0]				V14GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R23	0	1	0	1	1	1	R/W	x	V17GAM[3:0]				V16GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R24	0	1	1	0	0	0	R/W	x	V19GAM[3:0]				V18GAM[3:0]			
							1/0		1	0	0	0	1	0	0	0
R30	0	1	1	1	1	0	R/W	x	DBV[7:0]							
							1/0		1	1	1	1	1	1	1	1
R32	1	0	0	0	0	0	W	x	X	X	BCTL	X	DD	BL	X	X
							0		X	X	1	X	1	1	X	X

R33	1	0	0	0	0	1	R	x	X	X	BCTL	X	DD	BL	X	X
							1		X	X	1	X	1	1	X	X
R36	1	0	0	1	0	0	W	x	CMB[7:0]							
							0		0	0	0	0	0	0	0	0
R37	1	0	0	1	0	1	R	x	CMB[7:0]							
							1		0	0	0	0	0	0	0	0
R38	1	0	0	1	1	0	W	x	PWM_DIV[7:0]							
							0		0	0	0	0	1	1	1	1
R39	1	0	0	1	1	1	W	x	THRES_MOV[3:0]				THRES_STILL[3:0]			
							0		1	1	0	0	1	1	0	0
R40	1	0	1	0	0	0	W	x	X	X	X	X	THRES_UI[3:0]			
							0		X	X	X	X	1	1	0	0
R41	1	0	1	0	0	1	W	x	Min-DTH_MOV[3:0]				Min-DTH_STILL[3:0]			
							0		0	1	1	0	0	1	0	1
R42	1	0	1	0	1	0	W	x	X	X	X	X	Min-DTH_UI[3:0]			
							0		X	X	X	X	0	1	0	0
R43	1	0	1	0	1	1	W	x	DIM_OPT2[3:0]				X	DIM_OPT1[2:0]		
							0		0	1	1	1	X	1	0	0

Register R0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	FRAD1	FRAD0	DITHB
Default	0	0	0	0	0	0	0	0

DITHB: Dithering control bit.

DITHB="1", Dithering function is disabled, (7-bits resolution, truncation last 1-bits of the input data)

DITHB="0", Dithering function is enabled, (Pseudo 8-bits resolution). (Default)

FRAD[1:0]: Odd / Even frame advance control. FRAD should be correctly configured if the HBP of even-frame and odd-frame of incoming data are different. There are three examples for FRAD setting reference.

Example 1: If HBP in odd-frame is 21 and HBP in even-frame is 21, then FRAD should be set to 0 and HDL should be set to 21.

Example 2: If HBP in odd-frame is 21 and HBP in even-frame is 22 (odd frame advance), then FRAD should be set to 1 and HDL should be set to 21.

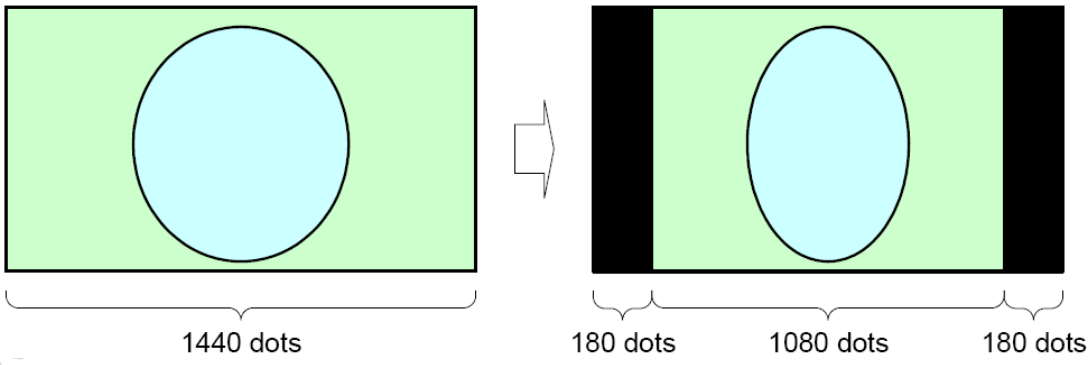
Example 3: If HBP in odd-frame is 21 and HBP in even-frame is 20 (even frame advance), then FRAD should be set to 2 and HDL should be set to 20.

FRAD1	FRAD0	Descriptions	Notes
0	0	Default	Odd/Even frame Tstv are the same
0	1	Odd frame advance	Even frame Tstv = HDL setting +1
1	0	Even frame advance	Odd frame Tstv = HDL setting +1
1	1	Reserved	Reserved

NFSEL: Narrow display mode selection bit.

NFSEL="1": Narrow display format is enabled.

NFSEL="0": Normal display is selected. (Default)



FPOL: VCOM polarity inverse control bit.

FPOL="1", VCOM inverse polarity.

FPOL="0", VCOM normal polarity. (Default)

CLKPOL: DCLK polarity control bit.

CLKPOL="1": Data is latched at DCLK falling edge.

CLKPOL="0": Data is latched at DCLK rising edge. (Default)

VSDPOL: VSD polarity control bit.

VSDPOL="1": VSD positive polarity.

VSDPOL="0": VSD negative polarity. (Default)

HSDPOL: HSD polarity control bit.

HSDPOL="1": HSD positive polarity.

HSDPOL="0": HSD negative polarity. (Default)

Register R1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CABC_MODE[1]	CABC_MODE[0]	x	LHL	STB	GRB	SHRL	UPDN
Default	0	0		1	1	1	1	1

UPDN: Gate driver up/down scan direction control

UPDN="1", Gate signal shift from up to down, L1 (1st line)→ L2 → … →L543→L544 (Last line) (Default)

UPDN="0", Gate signal shift from down to up, L544 (1st line) →L543→ … →L2→L1 (Last line)

SHRL: Right/Left sequence control of source driver.

SHLR="1", Shift right: First data=S1 →S2→S3 … →S720=Last data (Default)

SHLR="0", Shift left: Last data=S1,←S2←S3 … ←S720=First data

GRB: Global reset bit.

GRB="1", Normal operation. (Default)

GRB="0", the controller is in reset state.

STB: Standby mode selection bit.

STB="1", Normal operation. (Default)

STB="0", Standby mode.

LHL: Line/Half-Line inversion selection bit.

LHL="1", Half line inversion. (Default)

LHL="0", Line inversion.

CABC_MODE1/0: CABC operation mode selection

CABC_MODE[1:0]	Description
0	CABC OFF
1	User Interface Image
2	Still Picture
3	Moving Image

Register R2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	VFBSEL[1:0]		DRV_FREQ	PWM_DUTY[2:0]			SHDB
Default	x	0	1	0	0	1	1	0

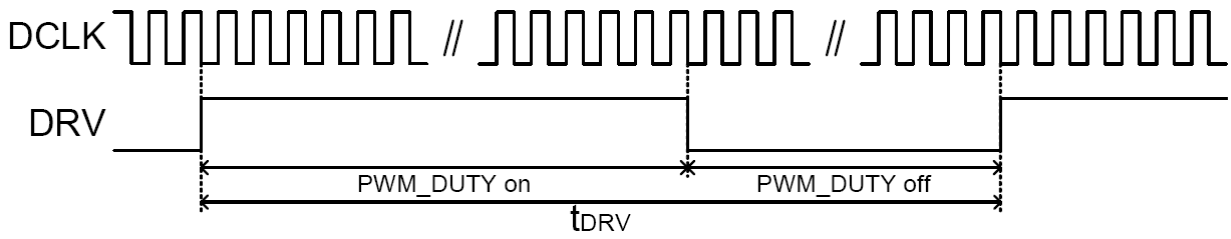
SHDB: Shut down the back light power converter.

SHDB="1", the back light power converter is controlled by STB's power on/off sequence

SHDB="0", the back light power converter is off. (Default)

PWM_DUTY[2:0]: PWM duty cycle selection for back light power converts

PWM_DUTY[2:0]	PWM Duty Cycle
000	50%
001	60%
010	65%
011	70%(Default)
100	75%
101	80%
110	85%
111	90%



DRV_FREQ : DRV signal frequency setting

DRV_FREQ="1", DRV frequency is DCLK/64.

DRV_FREQ="0", DRV frequency is DCLK/32. (Default)

VFBSEL[1:0] : FB voltage adjustable for DC-DC feedback threshold

VFBSEL[1:0]	Feedback threshold Voltage	Unit
00	0.75	Volt
01	0.60 (Default)	
10	0.45	
11	0.30	

Register R3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LED_ON_CYCLE[3:0]				LED_ON_RATIO[3:0]			
Default	0	1	1	1	1	1	1	1

LED_ON_RATIO[3:0]: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

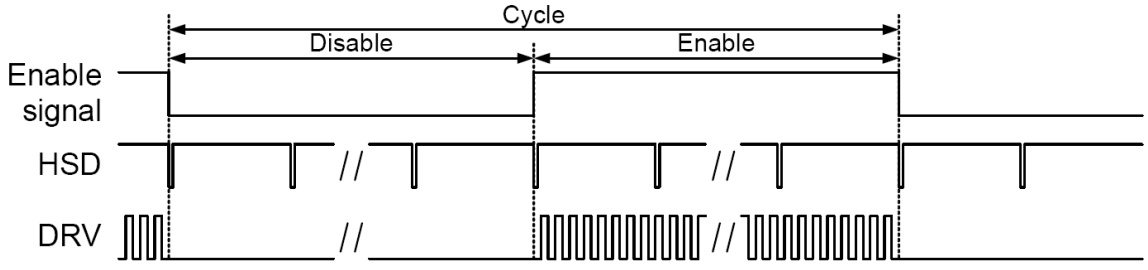
LED_ON_RATIO[3:0]	Value
4'b0000	1/16
4'b0001	2/16
4'b0010	3/16
4'b0011	4/16
4'b0100	5/16
4'b0101	6/16
4'b0110	7/16
4'b0111	8/16

LED_ON_RATIO[3:0]	Value
4'b1000	9/16
4'b1001	10/16
4'b1010	11/16
4'b1011	12/16
4'b1100	13/16
4'b1101	14/16
4'b1110	15/16
4'b1111 (default)	16/16

LED_ON_CYCLE[3:0]: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE[3:0]	Value
4'b0000	1
4'b0001	2
4'b0010	3
4'b0011	4
4'b0100	5
4'b0101	6
4'b0110	7
4'b0111(default)	8

LED_ON_CYCLE[3:0]	Value
4'b1000	9
4'b1001	10
4'b1010	11
4'b1011	12
4'b1100	13
4'b1101	14
4'b1110	15
4'b1111	16



16*LED_ON_CYCLE=LED_ON_CYCLE*(LED_ON_RATIO*16)+LED_ON_CYCLE*(16-LED_ON_RATIO*16)
(Cycle) **(Enable)** **(Disable)** Unit:HSD

Register R4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DDL[7:0]							
Default	0	0	1	0	1	0	0	0

DDL[7:0]: Select the HSD signal to 1'st input data delay timing.

DDL[7:0]	DDL Function	UNIT
8'h00	Setting prohibited	DCLK
8'h01	Setting prohibited	
…	…	
8'h24	Setting prohibited	
8'h25	37	
8'h26	38	
…	…	
8'h28	40(Default setting for Parallel mode)	
8'h29	41	
…	…	
8'h78	120(Default setting for Serial mode)	
8'h79	121	
…	…	
8'hFF	255	

Register R5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	HDL[4:0]				
Default	x	x	x	0	1	0	0	0

HDL[4:0]: Select the Gate start pulse output delay timing.

HDL[4:0]	HDL Function	UNIT
5'h00	Setting prohibited	HSD
…	…	
5'h05	5	
…	…	
5'h08	8 (default)	
…	…	
5'h1F	31	

Register R6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOMH_OTP	VCOMH[6]	VCOMH[5]	VCOMH[4]	VCOMH[3]	VCOMH[2]	VCOMH[1]	VCOMH[0]
Default	0	1	0	1	0	0	1	1

VCOMH[6:0]: Set the VCOMH voltage (20mV/LSB).

VCOMH[6:0]	VCOMH Voltage	Unit
7'b00h	2.46	Volt
7'b01h	2.48	
…	…	
7'b1Bh	3	
7'b1Ch	3.02	
…	…	
7'b53h	4.12(default)	
7'b54h	4.14	
…	…	
7'b7Fh	5	

VCOMH_OTP:

VCOMH_OTP =”1”, VCOMH is switched to the 3-wire register memory when the user wants to adjust the VCOMH level.

VCOMH_OTP =”0”, VCOMH is read from OTP memory. (Default)

Register R7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOML_OTP	VCOML[6]	VCOML[5]	VCOML[4]	VCOML[3]	VCOML[2]	VCOML[1]	VCOML[0]
Default	0	0	1	1	1	1	1	0

VCOML[6:0]: Set the VCOML voltage (20mV/LSB).

VCOML[6:0]	VCOML Voltage	Unit
7’b00h	-0.46	Volt
7’b01h	-0.48	
…	…	
7’b3Dh	-1.68	
7’b3Eh	-1.70(default)	
…	…	
7’b4Dh	-2	
7’b4Eh	-2.02	
…	…	
7’b7Fh	-3	

VCOML_OTP:

VCOML_OTP =”1”, VCOML is switched to the 3-wire register memory when the user wants to adjust the VCOMH level.

VCOML_OTP =”0”, VCOML is read from OTP memory. (Default)

Register R8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BRI[7:0]							
Default	0	1	0	0	0	0	0	0

BRI[7:0]: Brightness level setting, the gain changes 1 step/bit

BRI[7:0]	Brightness Offset
8’h00	Dark (-64)
8’h01	-63
…	…
8’h40	Center (0, Default)
…	…
8’hFF	Bright (+191)

Register R9

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CON[7:0]							
Default	0	1	0	0	0	0	0	0

CON[7:0]: Contrast level setting, the gain changes (1/64)/bit

CON[7:0]	Contrast Gain
8'h00	0
8'h01	1/64
…	…
8'h40	1 (Default)
…	…
8'hFF	3.984

Register R10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_BRI_R[6:0]						
Default	x	1	0	0	0	0	0	0

SUB_BRI_R[6:0]: Red sub-pixel brightness level setting, setting accuracy: 1 step/bit

SUB_BRI_R[6:0]	Red Brightness Offset
7'h00	Dark (-64)
7'h01	-63
…	…
7'h40	Center (0) (Default)
…	…
7'h7F	Bright (+63)

Register R11

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_CON_R[6:0]						
Default	x	1	0	0	0	0	0	0

SUB_CON_R[6:0]: Red sub-pixel contrast level setting, the gain changes (1/256)/bit

SUB_CON_R[6:0]	Red Contrast Gain
7'h00	0.75
7'h01	0.75+ 1/256
…	…
7'h40	1 (Default)
…	…
7'h7F	1.246

Register R12

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_BRI_B[6:0]						
Default	x	1	0	0	0	0	0	0

SUB_ BRI _B[6:0]: Blue sub-pixel brightness level setting, setting accuracy: 1 step/bit

SUB_BRI_B[6:0]	Blue Brightness Offset
7'h00	Dark (-64)
7'h01	-63
…	…
7'h40	Center (0) (Default)
…	…
7'h7F	Bright (+63)

Register R13

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	SUB_CON_B[6:0]						
Default	x	1	0	0	0	0	0	0

SUB_CON_B[6:0]: Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

SUB_CON_B[6:0]	Blue Contrast Gain
7'h00	0.75
7'h01	0.75+ 1/256
…	…
7'h40	1 (Default)
…	…
7'h7F	1.246

Register R14

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CABC_BRI1	CABC_BRI0	V2GAM[3:0]				GAMEN	x
Default	0	1	1	0	0	0	1	-

GAMMA adjustment enable control bit.(adjustable voltage for V2-V9 and V12-V19)

GAMEN="1", Gamma correction enabled

GAMEN="0", Gamma correction disabled.

V2GAM[3:0]: V2 GAMMA voltage level setting. Adjust level = 20mV / Step

CABC_BRI[1:0]: CABC brightness level selection bits

CABC_BRI1	CABC_BRI0	brightness level
0	0	Low level
0	**1**	**Normal level (default)**
1	0	High level
1	1	Higher level

Register R15

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V4GAM[3:0]				V3GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V3GAM[3:0]: V3 GAMMA voltage level setting. Adjust level = 20mV / Step

V4GAM[3:0]: V4 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R16

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V6GAM[3:0]				V5GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V5GAM[3:0]: V5 GAMMA voltage level setting. Adjust level = 20mV / Step

V6GAM[3:0]: V6 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R17

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V8GAM[3:0]				V7GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V7GAM[3:0]: V7 GAMMA voltage level setting. Adjust level = 20mV / Step

V8GAM[3:0]: V8 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R18

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	V9GAM[3:0]			
Default	x	x	x	x	1	0	0	0

V9GAM[3:0]: V9 GAMMA voltage level setting. Adjust level = 20mV / Step

VxGAM[3:0]	Gamma Voltage	Unit	Note
4'h0	+160	mV	Refer to the Gamma Table for the default voltage level of V2~ V9
4'h8	VxGAM[3:0] (Default)		
4'hF	-140		

Register R19

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	VGL_SEL[1:0]		VGH_SEL[1:0]	
Default	x	x	x	x	1	1	1	1

VGH_SEL[1:0]: VGH output voltage selection

VGH_SEL[1:0]	VGH Voltage	Unit
2'b00	12	Volt
2'b01	13	
2'b10	14	
2'b11	15 (default)	

VGL_SEL[1:0]: VGL output voltage selection

VGL_SEL[1:0]	VGL Voltage	Unit
2'b00	-7	Volt
2'b01	-8	
2'b10	-9	
2'b11	-10 (default)	

Register R20

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRMEN[7:0]							
Default	0	0	0	0	0	0	0	0

TRMEN[7:0]: VCOMH and VCOML trim function control register.

Write the following command sequentially to enable the VCOMH[6:0] and VCOML[6:0] trim function.

Adjust VCOMH level:

Set TRMEN[7:0]=00H and write proper VCOMH[6:0] value by the 3-wire SPI interface.

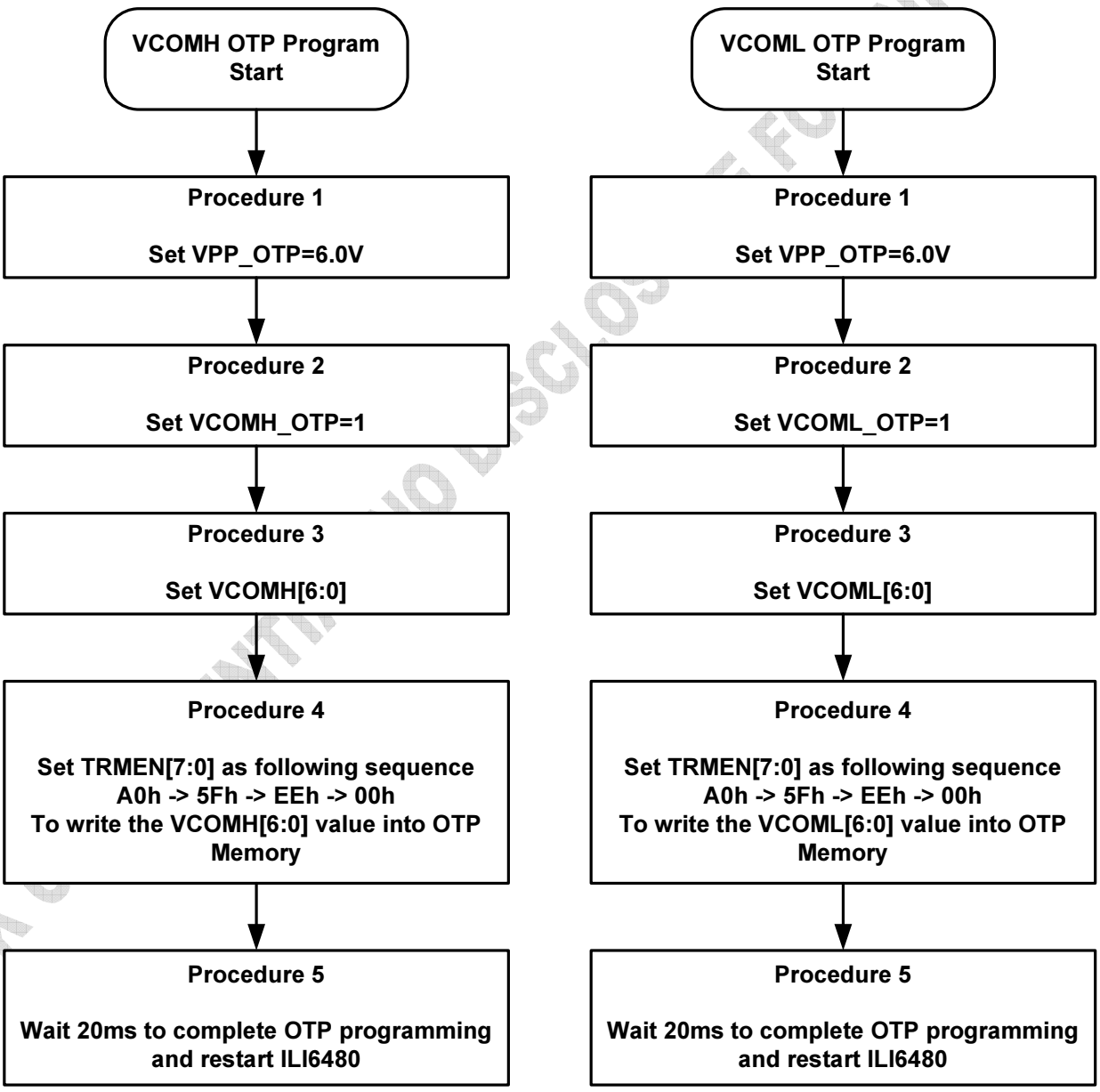
Programming the VCOMH[6:0] value into OTP memory:

Set TRMEN[7:0] as following sequence A0H->5FH->EEH->00H

VCOMH_OTP will be clear to 0b after the programming procedure.

Note:

1. ***The trim block can be written for only 2 times. Trim command exceed the limit may cause the VCOMH/VCOML output unknown value.***
2. ***VCOMH_OTP or VCOML_OTP will be clear to 0b after the programming procedure.***



Register R21

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V13GAM[3:0]				V12GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V12GAM[3:0]: V12 GAMMA voltage level setting. Adjust level = 20mV / Step

V13GAM[3:0]: V13 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R22

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V15GAM[3:0]				V14GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V14GAM[3:0]: V14 GAMMA voltage level setting. Adjust level = 20mV / Step

V15GAM[3:0]: V15 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R23

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V17GAM[3:0]				V16GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V16GAM[3:0]: V16 GAMMA voltage level setting. Adjust level = 20mV / Step

V17GAM[3:0]: V17 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R24

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	V19GAM[3:0]				V18GAM[3:0]			
Default	1	0	0	0	1	0	0	0

V18GAM[3:0]: V18 GAMMA voltage level setting. Adjust level = 20mV / Step

V19GAM[3:0]: V19 GAMMA voltage level setting. Adjust level = 20mV / Step

Register R30 (Read/Write Display Brightness Value)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DBV[7:0]							
Default	1	1	1	1	1	1	1	1

DBV[7:0]: This command is used to adjust the brightness value of the display.PWM_OUT signal's pulse duty is selected from 256 values between 8'hFF and 8'h00 to adjust the LED brightness..

When this register is read back, the LED brightness data for PWM_OUT signal is read by baseband and basenabd can adjust the backlight brightness based the read back DBV value.

Register R32 (Write CTRL Display)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	BCTL	x	DD	BL	x	x
Default	x	x	1	x	1	1	x	x

X: don't care

BCTRL: Brightness Control Block On/Off.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting. When the CABC is enabled, the dimming function is controlled by CABC block automatically.

DD	Description
0	Display Dimming OFF (Changes immediately)
1	Display Dimming On (Changes gradually base on the R43 register setting)

BL: Backlight Control (PWM_OUT signal) On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

Register R33 (Read CTRL Display)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	BCTL	x	DD	BL	x	x
Default	x	x	1	x	1	1	x	x

X: don't care

This command is used to read the CTRL register.

Register R36 (Write CABC Minimum Brightness)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMB[7:0]							
Default	0	0	0	0	0	0	0	0

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: this register is used to limit the brightness reduction. When CABC function is enabled, the display brightness can't be reduced to exceed the CABC minimum brightness setting.
When the CABC function is disabled (R34h=00h), CABC minimum brightness setting is ignored and user can set the DBV[7:0] smaller than CMB[7:0] value.

Register R37 (Read CABC Minimum Brightness)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMB[7:0]							
Default	0	0	0	0	0	0	0	0

This command is used to read the minimum brightness value of the display for CABC function.

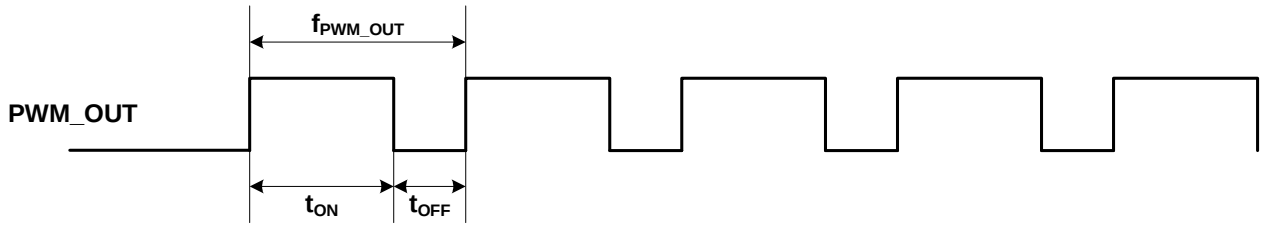
Register R38 (CABC Control 1)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWM_DIV[7:0]							
Default	0	0	0	0	1	1	1	1

PWM_DIV[7:0]: PWM_OUT output frequency control. The PWM_OUT frequency can be calculated by the following equation and the duty is based on the CABC result.

$$f_{pwm\_out} = \frac{9MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0]	f_{PWM_OUT}
8'0h	31.37 KHz
8'1h	15.69 KHz
8'2h	10.46KHz
8'3h	7.843 KHz
…	…
8'Fh	2.026KHz
…	…
8'FCh	140Hz
8'FDh	139Hz
8'FEh	138Hz
8'FFh	137Hz



***Note**: The output frequency tolerance of internal frequency divider in CABC is ±10%*

Register R39 (CABC Control 2)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	THRES_MOV[3:0]				THRES_STILL[3:0]			
Default	1	1	0	0	1	1	0	0

THRES_MOV[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving picture mode.

This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

THRES_MOV[3:0]	Description
4’0h	99%
4’1h	98%
4’2h	96%
4’3h	94%
4’4h	92%
4’5h	90%
4’6h	88%
4’7h	86%

THRES_MOV[3:0]	Description
4’8h	84%
4’9h	82%
4’Ah	80%
4’Bh	78%
4’Ch	**76%**
4’Dh	74%
4’Eh	72%
4’Fh	70%

THRES_STILL[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode.

This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

THRES_STILL[3:0]	Description
4’0h	99%
4’1h	98%
4’2h	96%
4’3h	94%
4’4h	92%
4’5h	90%
4’6h	88%
4’7h	86%

THRES_STILL[3:0]	Description
4’8h	84%
4’9h	82%
4’Ah	80%
4’Bh	78%
4’Ch	**76%**
4’Dh	74%
4’Eh	72%
4’Fh	70%

Register R40 (CABC Control 3)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	THRES_UI[3:0]			
Default	x	x	x	x	1	1	0	0

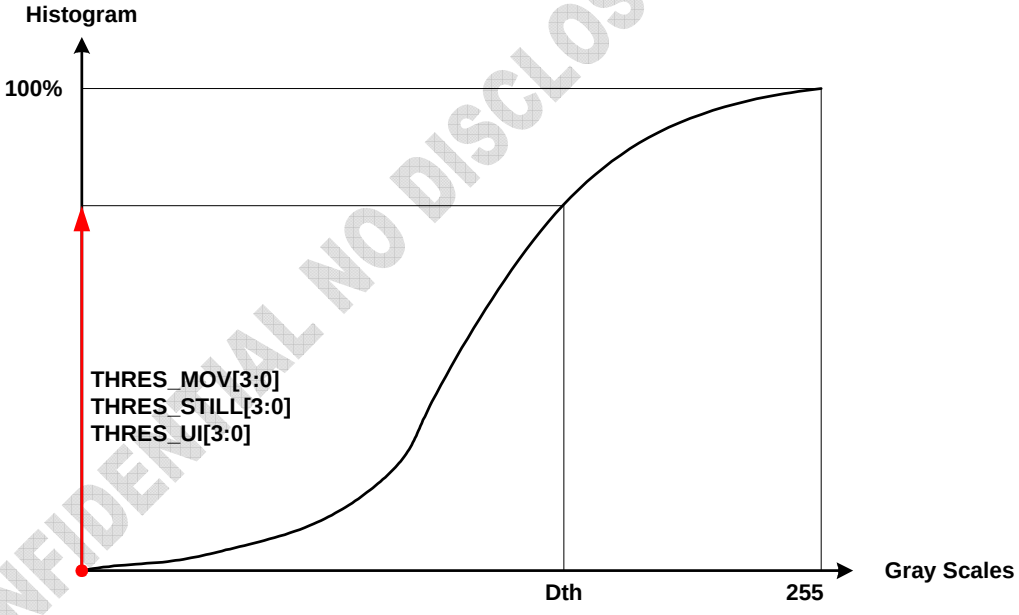
X: don't care

THRES_UI[3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode.

This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

THRES_UI[3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

THRES_UI[3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	**76%**
4'Dh	74%
4'Eh	72%
4'Fh	70%



Register R41 (CABC Control 4)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Min-DTH_MOV[3:0]				Min-DTH_STILL[3:0]			
Default	0	1	1	0	0	1	0	1

Min-DTH_MOV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not accpetable.

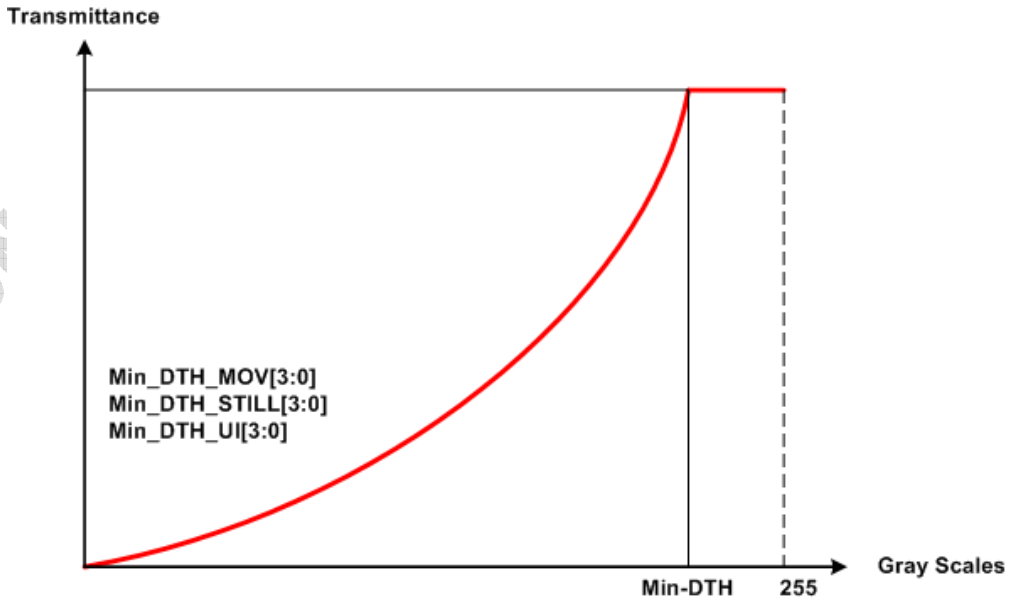
Min-DTH_MOV[3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	**200**
4'7h	196

Min-DTH_MOV[3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

Min-DTH_STILL[30]: This parameter is used set the minimum limitation of grayscale threshold value in STILL image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not accpetable.

Min-DTH_STILL[3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	**204**
4'6h	200
4'7h	196

Min-DTH_STILL[3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164



Register R42 (CABC Control 5)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	x	x	x	x	Min-DTH_UI[3:0]			
Default	x	x	x	x	0	1	0	0

X: don't care

DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in user interface (UI) mode This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not accpetable.

Min-DTH_UI[3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	**236**
4'5h	232
4'6h	228
4'7h	224

Min-DTH_UI[3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

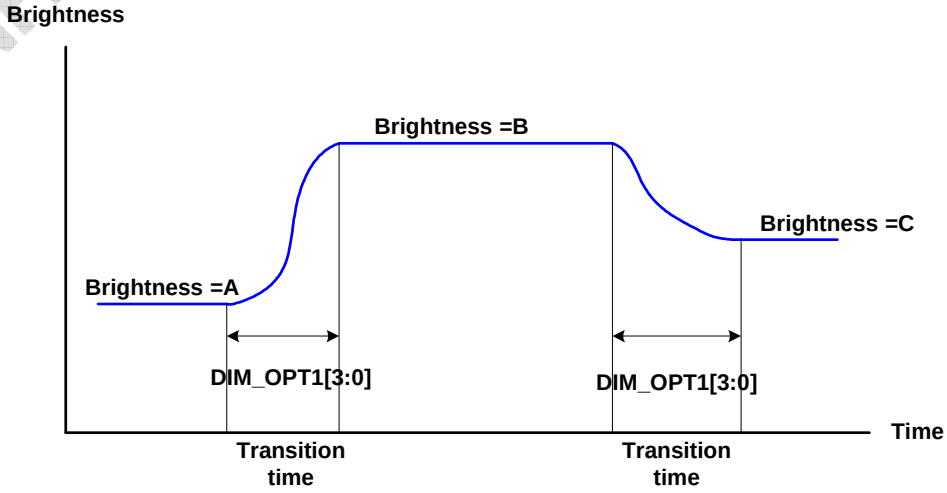
Register R43 (CABC Control 6)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIM_OPT2[3:0]				x	DIM_OPT1[2:0]		
Default	0	1	1	1	x	1	0	0

X: don't care

DIM_OPT1[2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM_OPT1[2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	**8 frames**
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames



DIM_OPT2[3:0]: This parameter is used to set the threshold of brightness change.

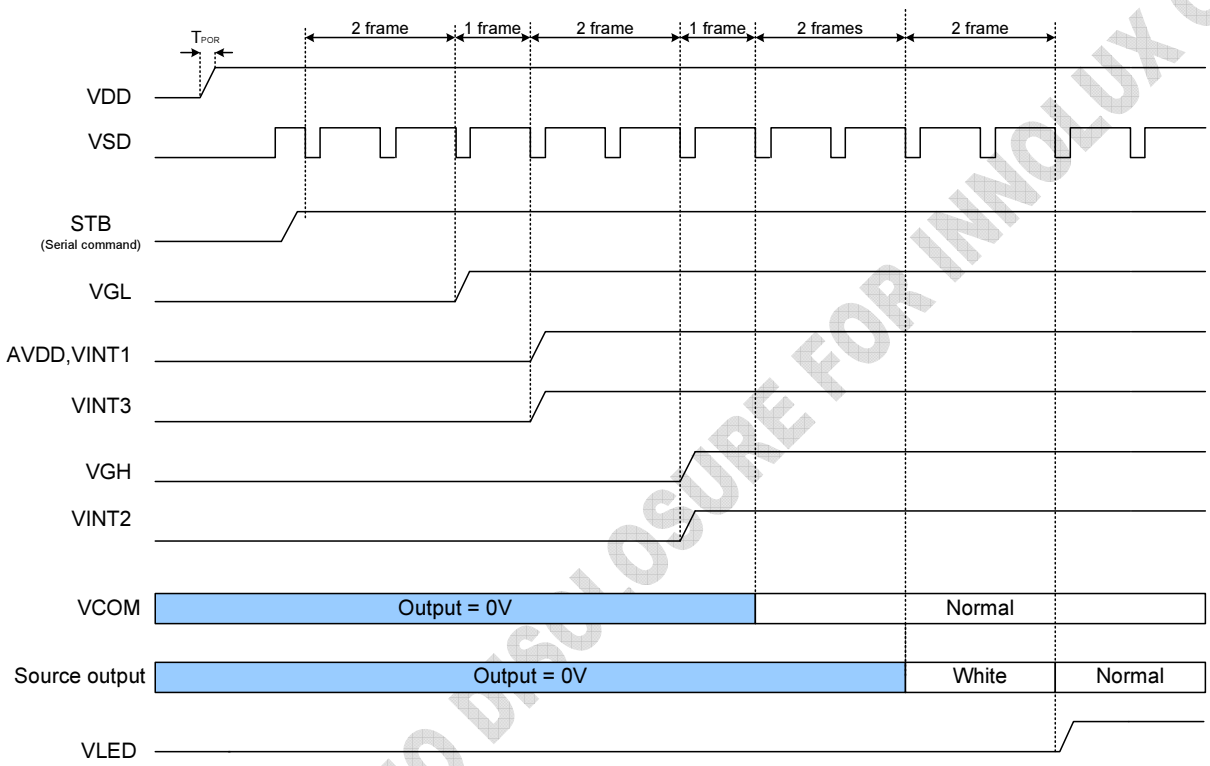
When the brightness transition difference is smaller than **DIM_OPT2[2:0]**, the brightness transition will be ignored. For example:

If | brightness B – brightness A| < DIM_OPT2[2:0], the brightness transition will be ignored and keep the brightness A.

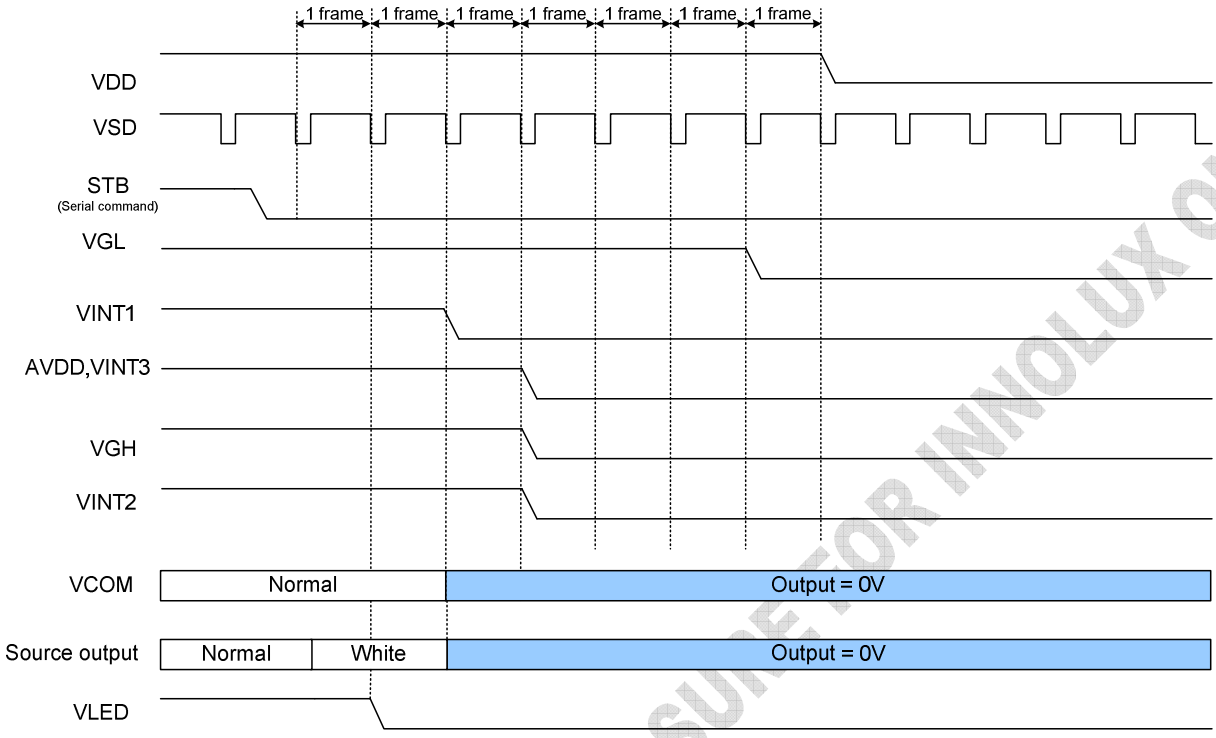
9. Power On/Off Sequence

In order to power on /off ILI6480B correctly, please follow the following recommended power on /off sequence.

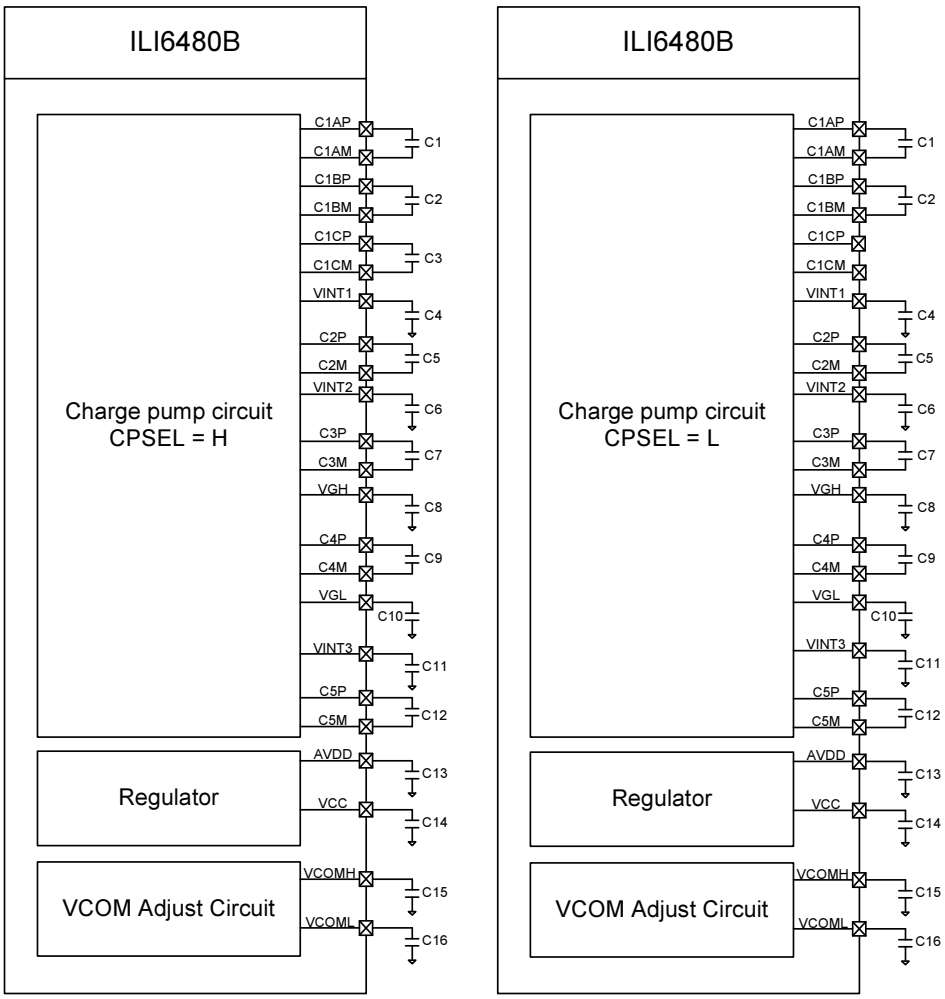
9.1. Power On Sequence



9.2. Power Off Sequence



9.3. Charge-pump Circuit Connection



Component	Value	Voltage proof
C1	2.2uF	6V
C2	2.2uF	6V
C3	2.2uF	6V
C4	4.7uF	10V
C5	1.0uF	16V
C6	2.2uF	16V
C7	1.0uF	16V
C8	2.2uF	25V
C9	1.0uF	16V
C10	2.2uF	16V
C11	4.7uF	10V
C12	2.2uF	6V
C13	4.7uF	10V
C14	2.2uF	6V
C15	4.7uF	10V
C16	4.7uF	10V

10. Input Data and Output Voltage

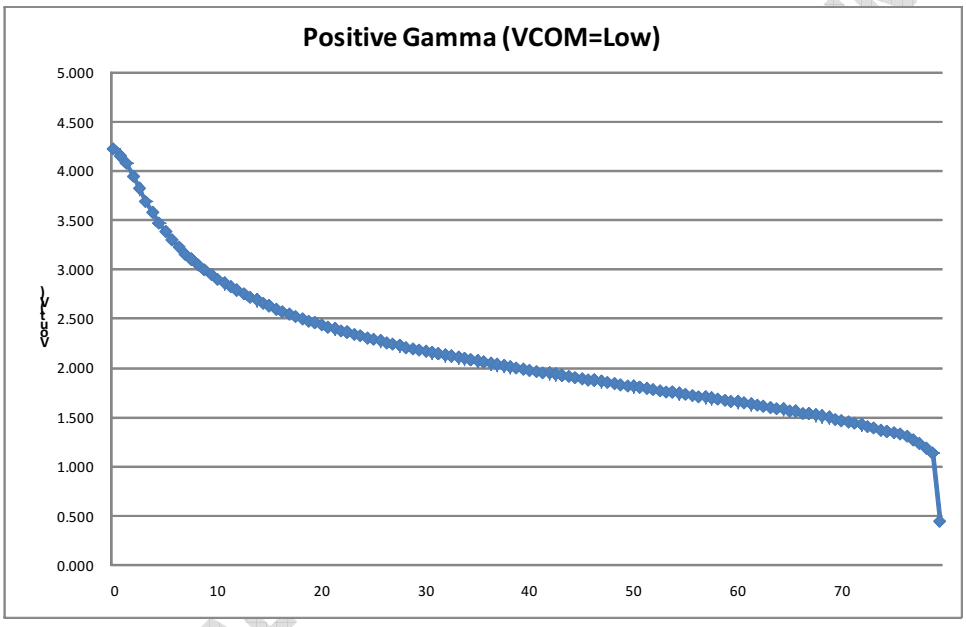
Source driver data output sequence can be control by “SHLR”.

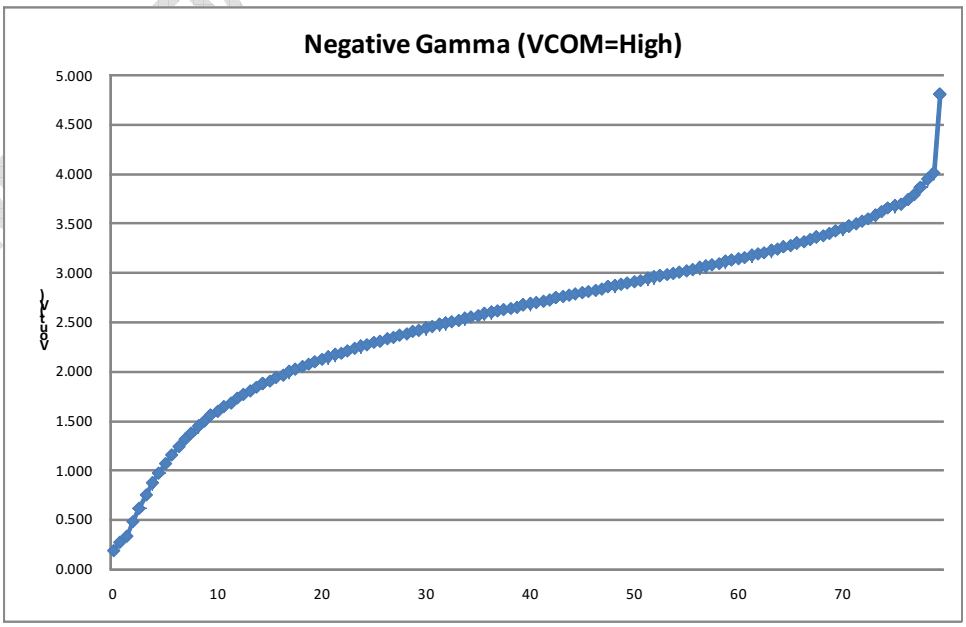
Output	S1	S2	S3	…	S718	S719	S720
SHLR =’1’	1st Data	→					Last Data
SHLR =’0’	Last Data	←					1st Data

Gate driver scan output sequence can be control by “UPDN”.

Output	G1	G2	G3	…	G542	G543	G544
UPDN =’1’	1st Data	→					Last Data
UPDN =’0’	Last Data	←					1st Data

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.





Input Data and Output Voltage Reference Table

Vno.	Data	VCOMOUT=H	Vno.	Data	VCOMOUT=H
V1	00H	0.185		40H	2.678
	01H	0.265		41H	2.694
	02H	0.331		42H	2.708
	03H	0.477		43H	2.723
	04H	0.609		44H	2.737
	05H	0.742		45H	2.753
	06H	0.861		46H	2.766
	07H	0.967		47H	2.782
	08H	1.065	V5	48H	2.795
	09H	1.153		49H	2.808
	0AH	1.237		4AH	2.821
	0BH	1.306		4BH	2.833
	0CH	1.373		4CH	2.849
	0DH	1.439		4DH	2.861
	0EH	1.492		4EH	2.877
	0FH	1.547		4FH	2.889
	10H	1.593		50H	2.905
	11H	1.638		51H	2.917
V2	12H	1.680		52H	2.933
	13H	1.725		53H	2.946
	14H	1.762		54H	2.961
	15H	1.799		55H	2.974
	16H	1.834		56H	2.989
	17H	1.868		57H	3.002
	18H	1.900		58H	3.017
	19H	1.932		59H	3.030
	1AH	1.961	V6	5AH	3.045
	1BH	1.990		5BH	3.058
	1CH	2.017		5CH	3.074
	1DH	2.043		5DH	3.089
	1EH	2.067		5EH	3.105
	1FH	2.091		5FH	3.121
	20H	2.115		60H	3.137
	21H	2.139		61H	3.152
	22H	2.160		62H	3.168
	23H	2.184		63H	3.184
V3	24H	2.205		64H	3.202
	25H	2.226		65H	3.218
	26H	2.247		66H	3.236
	27H	2.268		67H	3.254
	28H	2.287		68H	3.272
	29H	2.305		69H	3.291
	2AH	2.324		6AH	3.309
	2BH	2.342	V7	6BH	3.330
	2CH	2.361		6CH	3.349
	2DH	2.379		6DH	3.372
	2EH	2.398		6EH	3.394
	2FH	2.416		6FH	3.416
	30H	2.432		70H	3.439
	31H	2.451		71H	3.464
	32H	2.467		72H	3.489
	33H	2.482		73H	3.516
	34H	2.498		74H	3.544
	35H	2.514		75H	3.572
V4	36H	2.530		76H	3.611
	37H	2.546	V8	77H	3.650
	38H	2.562		78H	3.689
	39H	2.578		79H	3.739
	3AH	2.591		7AH	3.789
	3BH	2.607		7BH	3.865
	3CH	2.620		7CH	3.941
	3DH	2.636	V9	7DH	4.080
	3EH	2.649		7EH	4.301
	3FH	2.665	V10	7FH	4.800

Vno	Data	VCOMOUT=L	Vno.	Data	VCOMOUT=L
V20	00H	4.225		40H	1.975
	01H	4.151		41H	1.964
	02H	4.086		42H	1.954
	03H	3.951		43H	1.943
	04H	3.820		44H	1.933
	05H	3.689		45H	1.922
	06H	3.581		46H	1.911
	07H	3.472		47H	1.901
	08H	3.389	V16	48H	1.890
	09H	3.302		49H	1.879
	0AH	3.230		4AH	1.870
	0BH	3.160		4BH	1.859
	0CH	3.104		4CH	1.850
	0DH	3.045		4DH	1.839
	0EH	2.995		4EH	1.830
	0FH	2.947		4FH	1.819
	10H	2.903		50H	1.810
	11H	2.860		51H	1.799
V19	12H	2.825		52H	1.790
	13H	2.786		53H	1.779
	14H	2.751		54H	1.770
	15H	2.718		55H	1.759
	16H	2.687		56H	1.750
	17H	2.657		57H	1.739
	18H	2.629		58H	1.730
	19H	2.600		59H	1.721
	1AH	2.574	V15	5AH	1.710
	1BH	2.548		5BH	1.701
	1CH	2.524		5CH	1.690
	1DH	2.500		5DH	1.682
	1EH	2.478		5EH	1.671
	1FH	2.456		5FH	1.662
	20H	2.436		60H	1.651
	21H	2.417		61H	1.643
	22H	2.397		62H	1.630
	23H	2.377		63H	1.621
V18	24H	2.360		64H	1.608
	25H	2.342		65H	1.599
	26H	2.325		66H	1.586
	27H	2.307		67H	1.578
	28H	2.290		68H	1.565
	29H	2.272		69H	1.554
	2AH	2.259		6AH	1.541
	2BH	2.241	V14	6BH	1.530
	2CH	2.226		6CH	1.517
	2DH	2.211		6DH	1.506
	2EH	2.198		6EH	1.493
	2FH	2.182		6FH	1.480
	30H	2.169		70H	1.466
	31H	2.154		71H	1.453
	32H	2.140		72H	1.438
	33H	2.127		73H	1.422
	34H	2.116		74H	1.405
	35H	2.103		75H	1.390
V17	36H	2.090		76H	1.370
	37H	2.077	V13	77H	1.350
	38H	2.067		78H	1.331
	39H	2.054		79H	1.301
	3AH	2.043		7AH	1.275
	3BH	2.030		7BH	1.230
	3CH	2.020		7CH	1.185
	3DH	2.007	V12	7DH	1.110
	3EH	1.996		7EH	0.980
	3FH	1.986	V11	7FH	0.440

11. Wire resistance for each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance value(ohm)	Pin Name	Wiring resistance value(ohm)
VDD	<10	HSD	<50
PVDD	<3	VSD	<50
GND	<10	DCLK	<50
AGND	<10	DEN	<50
PGND	<3	DR0~DR7	<50
VDDIO	<10	DG0~DG7	<50
VPP_OTP	<10	DB0~DB7	<50
VCC	<10	CSB	<50
AVDD	<10	SDA	<50
VINT1	<5	SCL	<50
VINT2,3	<10	STB	<1000
C1AP/M	<5	GRB	<1000
C1BP/M	<5	HVDSL	<1000
C1CP/M	<5	UPDN	<1000
C2P/M	<10	SHLR	<1000
C3P/M	<10	PINCTL	<1000
C4P/M	<10	PSEL	<1000
C5P/M	<10	CPSEL	<1000
VCOM	<5	EXT_PWR	<1000
VCOMH	<10	CLKPOL	<1000
VCOML	<10	VSDPOL	<1000
VGH	<10	HSDPOL	<1000
VGL	<10	FPOL	<1000
DRV	<20	DITHB	<1000
FB	<50	SHDB	<1000
PWM_OUT	<50	LHL	<1000

12. DC Characteristic

12.1. Absolute Maximum Rating

Logic supply voltage, VDDIO	-0.5 to +5V
Analog supply voltage, AVDD	-0.3 to +7.0V
VGL	-16 to 0.3V
VGH~VGL	-0.3 to 35V
Operating Ambient Temperature, TA	-20 to ℃ 85℃
Storage Temperature, TSTR	-55℃ to+125℃

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Range

(GND=AGND=PGND=0V, TA= -20 to +85℃)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	
Digital interface supple Voltage	VDDIO	1.8	-	VDD	V	
Digital Input Voltage	Din	0	-	VDDIO	V	
OTP Supply Voltage	VPP_OTP	-	6	-	V	
VCOM AC Voltage	VCOMH - VCOML	2.96	-	6.2	V	

12.2. DC Electrical Characteristics

(VDDIO=VDD=3.0 to 3.6V, GND=AGND=PGND=0V, TA= -20 to 85 ℃)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Block Circuit						
Low Level Input Voltage	Vil	GND	-	0.3xVDDIO	V	Digital input pins
High Level Input Voltage	Vih	0.7xVDDIO	-	VDDIO	V	Digital input pins
Input Leakage Current	Ii	-	-	±1	uA	Digital input pins
Pull-high/low Impedance	Rin	-	200K	-	ohm	Digital control input pins VDDIO=3.3V
High Level Output Voltage	Voh	VDDIO-0.4	-	-	V	Digital input pins Ioh=400uA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins Iol=-400uA
Digital Stand-by Current	Idst	-	TBD	TBD	uA	Output are High-Z, all pins are default
Digital Operating Current	Icc	-	TBD	-	mA	DCLK=9MHz, Fld=17.28KHz (@ 24bit RGB mode), no load
Analog Block Circuit						
Analog Supply Voltage	AVDD	-	5.2	5.6	V	
GAMMA reference voltage	VDDA	-	5	-	V	
Step-up Circuit 1 Output Voltage	VINT1	5.8	-	-	V	
VCOMH Output Level	VCOMH	2.46		5	V	By VCOMH[6:0] setting
VCOML Output Level	VCOML	-3		-0.46	V	By VCOML[6:0] setting; VCOML>VINT3
Feed back voltage for PWM	VFB	0.25	0.6	0.8	V	DC-DC operating.
Base drive current for PWM	IDRV	-	20	-	mA	VDD=3.3V
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V ~ 0.5V & AVDD-0.5 ~ AVDD-0.1
		-	±15	±20	mV	Vo=0.5V ~ AVDD-0.5V
Dynamic Range of Ouput	Vdr	0.1	-	AVDD-0.1	V	S1 to S720
Low-level Output Current of VCOM	IOLC	-	TBD	-	mA	VCOMH=4V, VCOML=-1V VCOM output=-1V V.S. -0.1V
High-level Output Current of VCOM	IOHC	-	TBD	-	mA	VCOMH=4V, VCOML=-1V VCOM output=4V V.S. 3.1V
Source Low-level Output Current	IOLS	TBD	-	-	uA	S1 to S720; VO=0.1 V.S. 1V
Source High-level Output Current	IOHS	TBD	-	-	uA	S1 to S720; VO=4.9 V.S 4.0
Gate Low-level Output Current	IOLG	TBD	-	-	uA	G1 to G544; VO=VGL V.S. VGL+0.5
Gate High-level Output Current	IOHG	TBD	-	-	uA	G1 to G544; VO=VGH V.S. VGH-0.5
Analog Stand-by Current	Iast	-	-	100	uA	STB="L", all function are shutdown
Analog Operating Current	IDD	-	TBD	-	mA	DCLK=9MHz, Fld=17.28KHz (@ 24bit RGB mode), No load

13. AC Characteristic

13.1. Input signal characteristics

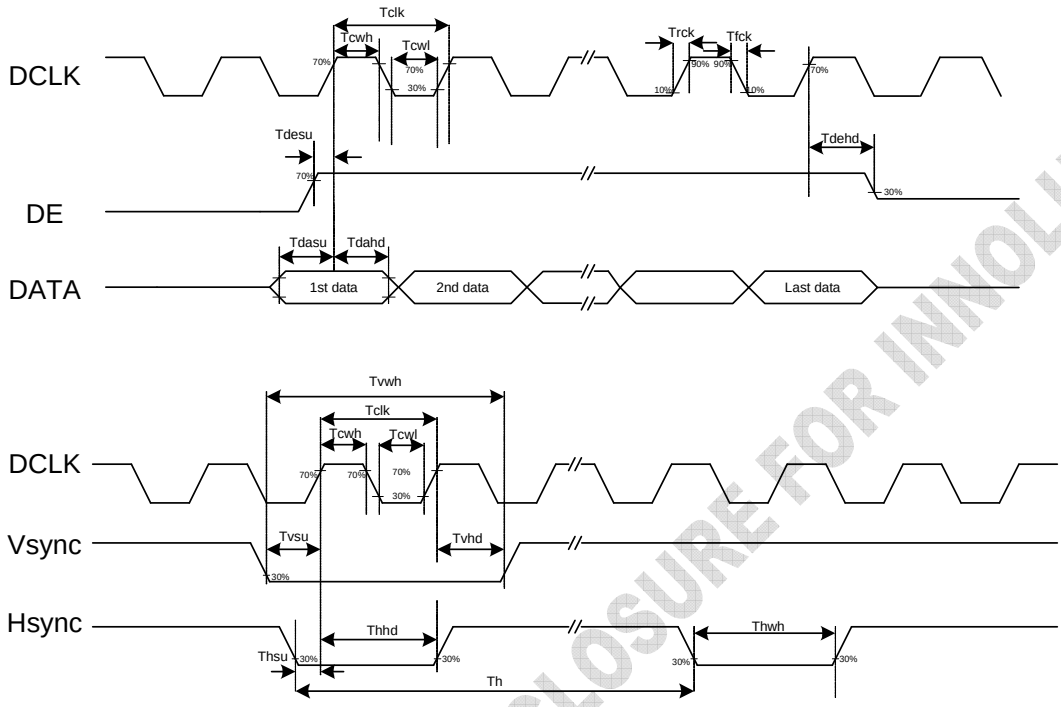
AC Electrical Characteristics (VDDIO=VDD=3.0 to 3.6v, GND=0V, TA=-20 to +85 ℃)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input Output timing						
DCLK clock time	Tclk	33.3	-	-	ns	DCLK=30MHz
DCLK clock low period	Tcwl	40	-	60	%	
DCLK clock high period	Tcwh	40	-	60	%	
Clock rising time	Trck	9	-	-	ns	
Clock falling time	Tfck	9	-	-	ns	
HSD width	Thwh	1	-	-	DCLK	
HSD period time	Th	55	60	65	us	
HSD setup time	Thsu	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
VSD width	Tvwh	1	-	-	Th	
VSD setup time	Tvsu	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
Data setup time	Tdasu	12	-	-	ns	
Data hold time	Tdahd	12	-	-	ns	
DE setup time	Tdesu	12	-	-	ns	
DE hold time	Tdehd	12	-	-	ns	
Source output setting time	Tsst	-	-	TBD	us	10% to 90% CL=60pF, RL=2Kohm
Gate output setting time	Tgst	-	-	TBD	ns	10% to 90%, CL=60pF
VCOM output setting time	Tcst	-	-	TBD	us	10% to 90%, CL=40nF, RL=50ohm
Time from VSD to 1st line data input	Tvs	3	8	31	Th	HV mode By HDL[4:0] setting
3-wire serial communication AC timing						
Serial clock	Tsck	200	-	-	ns	For SCL pin
SCL pulse low period	Tckl	40	-	60	%	
SCL pulse low period	Tckh	40	-	60	%	
Serial data setup time	Tisu	50	-	-	ns	
Serial data hold time	Tihd	50	-	-	ns	
Serial clock high/low	Tssw	50	-	-	ns	
CSB to VSD	Tcv	1			us	
CSB distinguish time	Tcd	400	-	-	ns	
CSB input setup time	Tcsu	50	-	-	ns	
CSB input hold time	Tchd	50	-	-	ns	

14. Waveform

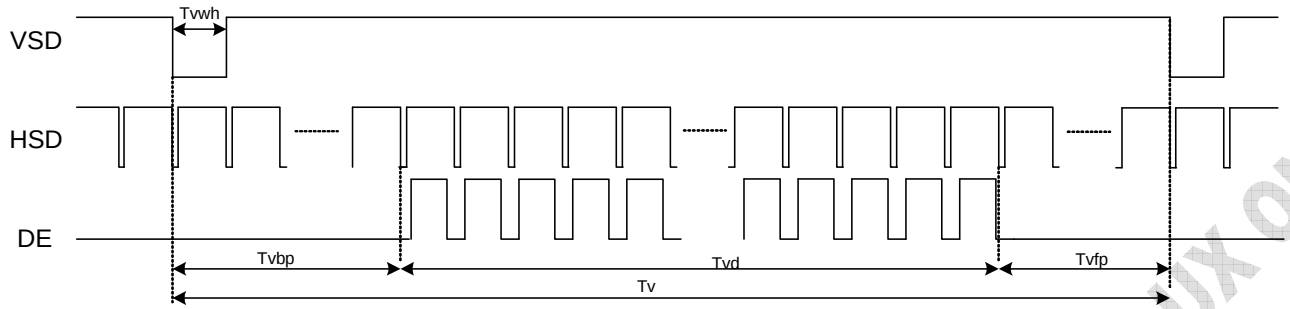
14.1. Timing Chart

14.1.1. Clock and Data Input Waveforms

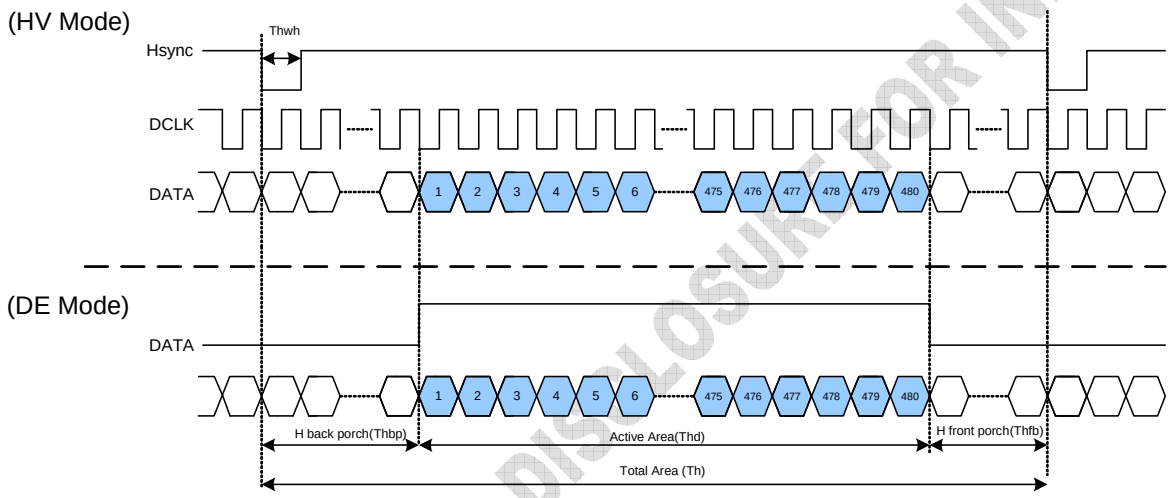


14.1.2. Data Input Format

Vertical input timing



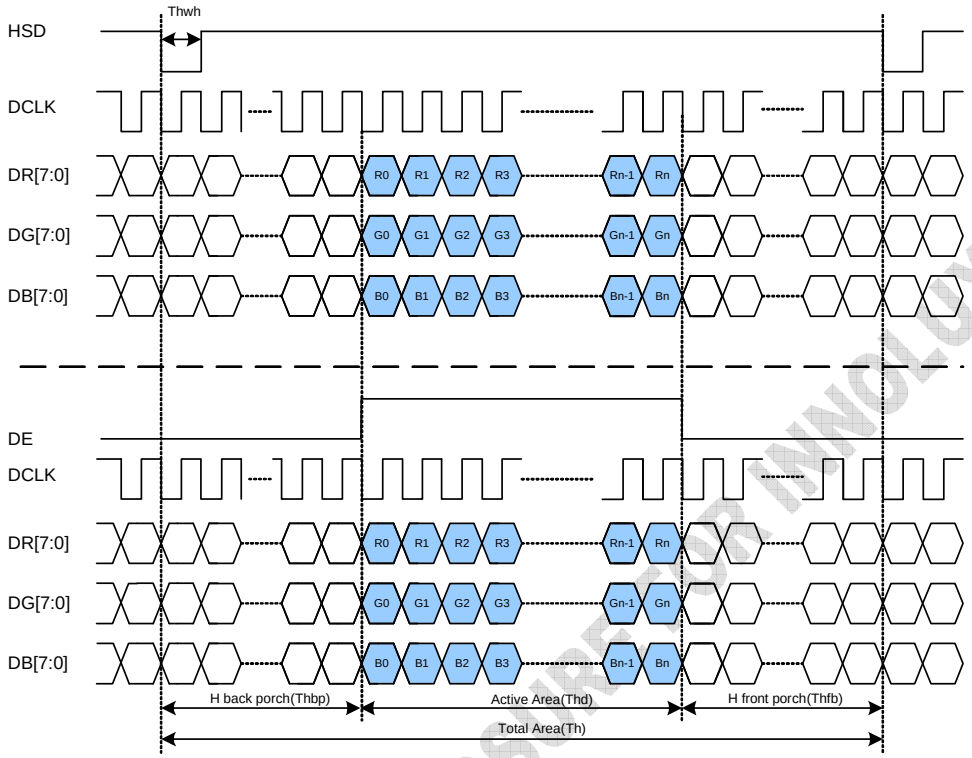
Serial 8-bit RGB Mode Data format



Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	24	27	30	MHz	
DCLK cycle time	Tclk	83	110	200	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
Time from HSD to source output	Thso	-	13	-	DCLK	
Time from HSD to gate output	Thgo	-	27	-	DCLK	
Time from HSD to gate output off	Thgz	-	3	-	DCLK	
Time from HSD to VCOM	Thvc	-	12	-	DCLK	

Parallel RGB Mode Data format

(HV Mode)



(DE Mode)

Parallel RGB input timign table

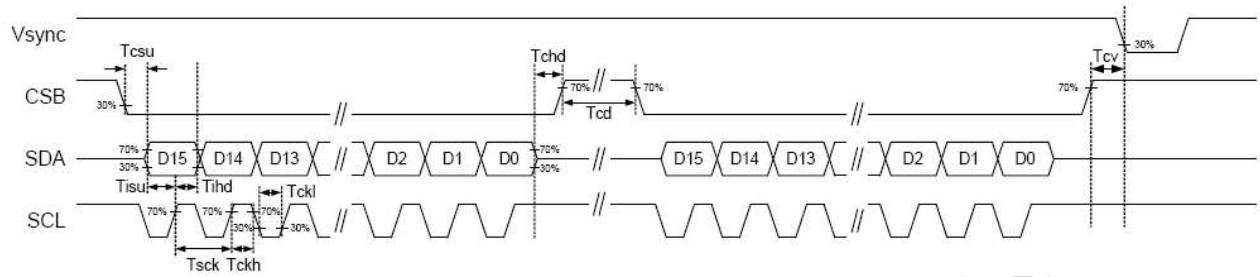
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	5	9	12	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	97	H
HSD period time	Th	520	525	800	DCLK
HSD display area	Thd		480		DCLK
HSD back porch	Thbp	36	40	255	DCLK
HSD front porch	Thfp	4	5	65	DCLK

Serial RGB input timign table

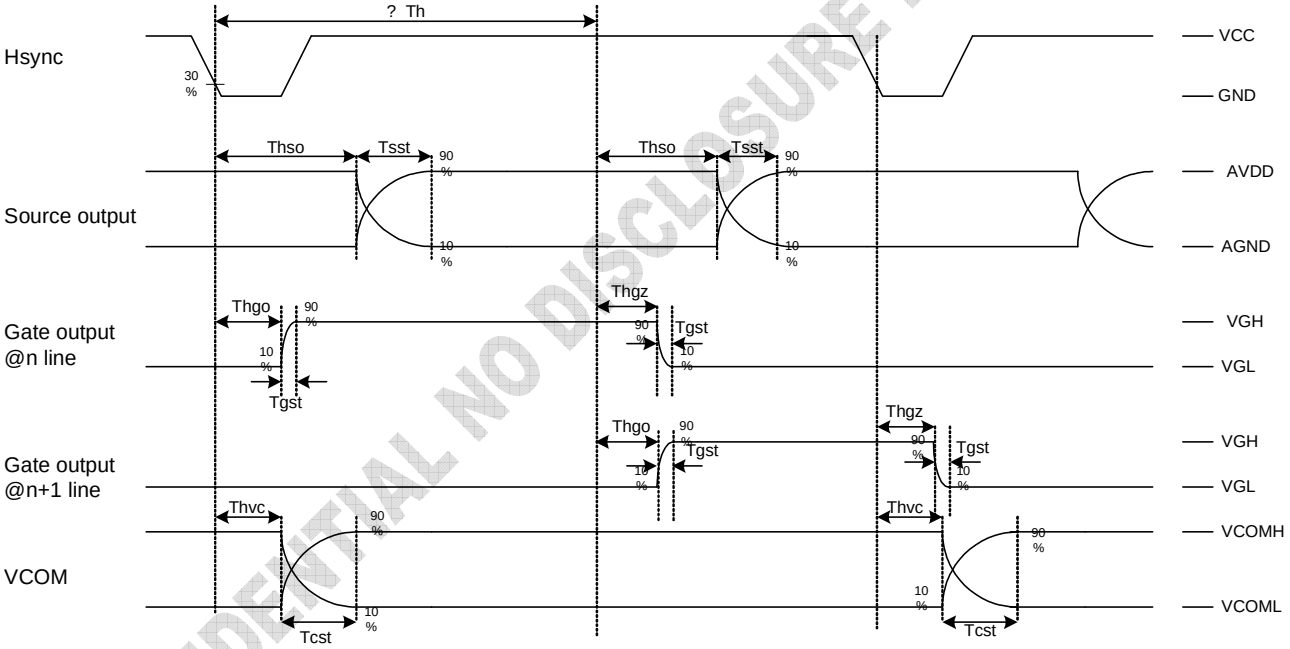
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	-	27	-	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	97	H
HSD period time	Th	-	1728	-	DCLK
HSD display area	Thd		1440		DCLK

HSD back porch	Thbp	-	120	-	DCLK
HSD front porch	Thfp	-	168	-	DCLK

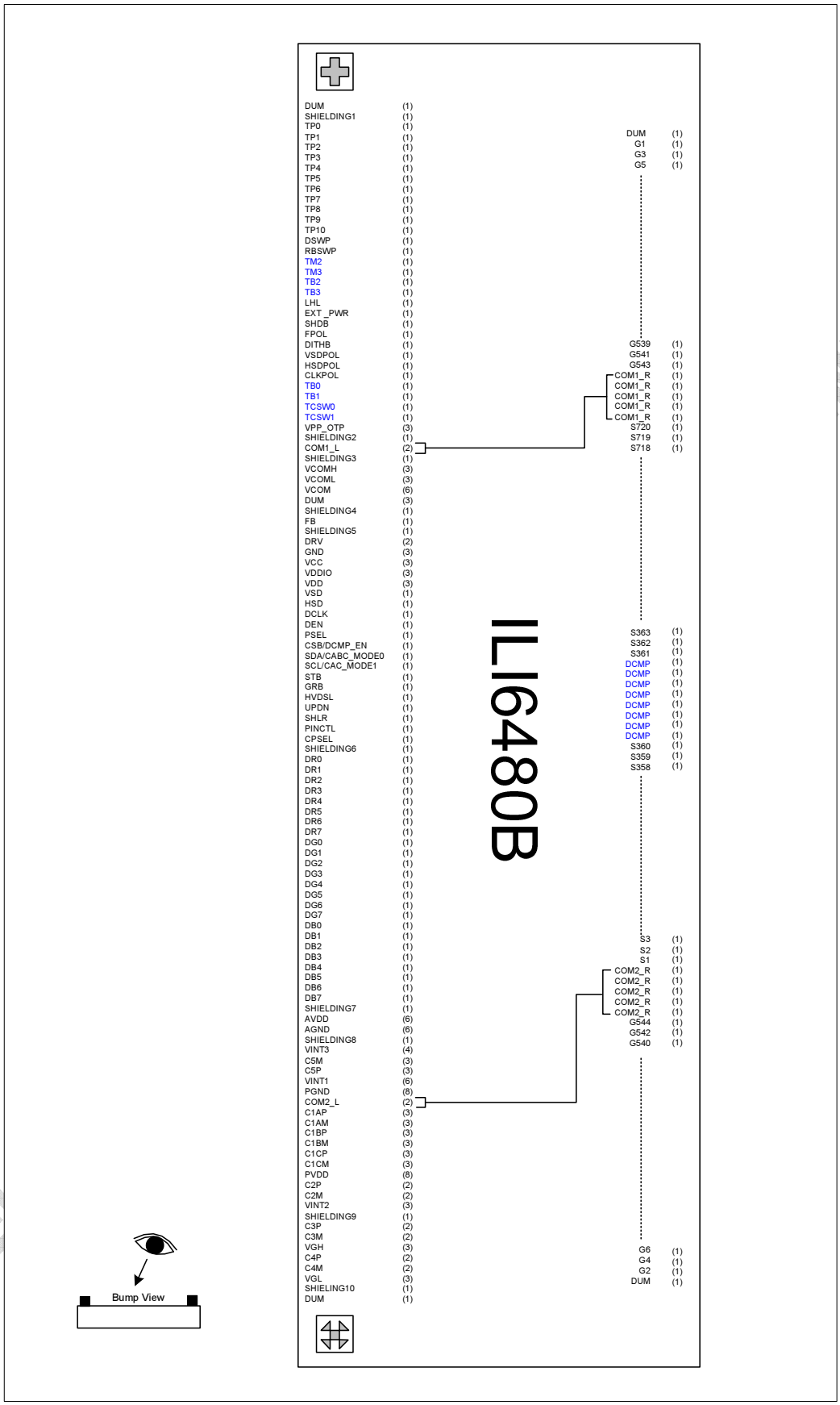
14.1.3. 3-wire Timing Diagram



14.1.4. Output Timing Diagram



15. Pin Assignment (IC Face View)



15.1. Pad Location

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1	DUM	-10941.5	-256	51	DUM	-5441.5	-256	101	DG6	58.5	-256
2	SHIELDING1	-10831.5	-256	52	DUM	-5331.5	-256	102	DG7	168.5	-256
3	TP0	-10721.5	-256	53	DUM	-5221.5	-256	103	DB0	278.5	-256
4	TP1	-10611.5	-256	54	SHIELDING4	-5111.5	-256	104	DB1	388.5	-256
5	TP2	-10501.5	-256	55	FB	-5001.5	-256	105	DB2	498.5	-256
6	TP3	-10391.5	-256	56	SHIELDING5	-4891.5	-256	106	DB3	608.5	-256
7	TP4	-10281.5	-256	57	DRV	-4781.5	-256	107	DB4	718.5	-256
8	TP5	-10171.5	-256	58	DRV	-4671.5	-256	108	DB5	828.5	-256
9	TP6	-10061.5	-256	59	GND	-4561.5	-256	109	DB6	938.5	-256
10	TP7	-9951.5	-256	60	GND	-4451.5	-256	110	DB7	1048.5	-256
11	TP8	-9841.5	-256	61	GND	-4341.5	-256	111	SHIELDING7	1158.5	-256
12	TP9	-9731.5	-256	62	VCC	-4231.5	-256	112	AVDD	1268.5	-256
13	TP10	-9621.5	-256	63	VCC	-4121.5	-256	113	AVDD	1378.5	-256
14	DSWP	-9511.5	-256	64	VCC	-4011.5	-256	114	AVDD	1488.5	-256
15	RBSWP	-9401.5	-256	65	VDDIO	-3901.5	-256	115	AVDD	1598.5	-256
16	TM2	-9291.5	-256	66	VDDIO	-3791.5	-256	116	AVDD	1708.5	-256
17	TM3	-9181.5	-256	67	VDDIO	-3681.5	-256	117	AVDD	1818.5	-256
18	TB2	-9071.5	-256	68	VDD	-3571.5	-256	118	AGND	1928.5	-256
19	TB3	-8961.5	-256	69	VDD	-3461.5	-256	119	AGND	2038.5	-256
20	LHL	-8851.5	-256	70	VDD	-3351.5	-256	120	AGND	2148.5	-256
21	EXT_PWR	-8741.5	-256	71	VSD	-3241.5	-256	121	AGND	2258.5	-256
22	SHDB	-8631.5	-256	72	HSD	-3131.5	-256	122	AGND	2368.5	-256
23	FPOL	-8521.5	-256	73	DCLK	-3021.5	-256	123	AGND	2478.5	-256
24	DITHB	-8411.5	-256	74	DEN	-2911.5	-256	124	SHIELDING8	2588.5	-256
25	VSDPOL	-8301.5	-256	75	PSEL	-2801.5	-256	125	VINT3	2698.5	-256
26	HSDPOL	-8191.5	-256	76	CSB/RESERVED	-2691.5	-256	126	VINT3	2808.5	-256
27	CLKPOL	-8081.5	-256	77	SDA/CABC_MODE0	-2581.5	-256	127	VINT3	2918.5	-256
28	TB0 (PWM_OUT)	-7971.5	-256	78	SCL/CABC_MODE1	-2471.5	-256	128	VINT3	3028.5	-256
29	TB1	-7861.5	-256	79	STB	-2361.5	-256	129	C5M	3138.5	-256
30	TCSW0	-7751.5	-256	80	GRB	-2251.5	-256	130	C5M	3248.5	-256
31	TCSW1	-7641.5	-256	81	HVDSL	-2141.5	-256	131	C5M	3358.5	-256
32	VPP_OTP	-7531.5	-256	82	UPDN	-2031.5	-256	132	C5P	3468.5	-256
33	VPP_OTP	-7421.5	-256	83	SHLR	-1921.5	-256	133	C5P	3578.5	-256
34	VPP_OTP	-7311.5	-256	84	PINCTL	-1811.5	-256	134	C5P	3688.5	-256
35	SHIELDING2	-7201.5	-256	85	CPSEL	-1701.5	-256	135	VINT1	3798.5	-256
36	COM1_L	-7091.5	-256	86	SHIELDING6	-1591.5	-256	136	VINT1	3908.5	-256
37	COM1_L	-6981.5	-256	87	DR0	-1481.5	-256	137	VINT1	4018.5	-256
38	SHIELDING3	-6871.5	-256	88	DR1	-1371.5	-256	138	VINT1	4128.5	-256
39	VCOMH	-6761.5	-256	89	DR2	-1261.5	-256	139	VINT1	4238.5	-256
40	VCOMH	-6651.5	-256	90	DR3	-1151.5	-256	140	VINT1	4348.5	-256
41	VCOMH	-6541.5	-256	91	DR4	-1041.5	-256	141	PGND	4458.5	-256
42	VCOML	-6431.5	-256	92	DR5	-931.5	-256	142	PGND	4568.5	-256
43	VCOML	-6321.5	-256	93	DR6	-821.5	-256	143	PGND	4678.5	-256
44	VCOML	-6211.5	-256	94	DR7	-711.5	-256	144	PGND	4788.5	-256
45	VCOM	-6101.5	-256	95	DG0	-601.5	-256	145	PGND	4898.5	-256
46	VCOM	-5991.5	-256	96	DG1	-491.5	-256	146	PGND	5008.5	-256
47	VCOM	-5881.5	-256	97	DG2	-381.5	-256	147	PGND	5118.5	-256
48	VCOM	-5771.5	-256	98	DG3	-271.5	-256	148	PGND	5228.5	-256
49	VCOM	-5661.5	-256	99	DG4	-161.5	-256	149	COM2_L	5338.5	-256
50	VCOM	-5551.5	-256	100	DG5	-51.5	-256	150	COM2_L	5448.5	-256

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
151	C1AP	5558.5	-256	201	DUM	11135	261	251	G100	10268	261
152	C1AP	5668.5	-256	202	G2	11101	121	252	G102	10251	121
153	C1AP	5778.5	-256	203	G4	11084	261	253	G104	10234	261
154	C1AM	5888.5	-256	204	G6	11067	121	254	G106	10217	121
155	C1AM	5998.5	-256	205	G8	11050	261	255	G108	10200	261
156	C1AM	6108.5	-256	206	G10	11033	121	256	G110	10183	121
157	C1BP	6218.5	-256	207	G12	11016	261	257	G112	10166	261
158	C1BP	6328.5	-256	208	G14	10999	121	258	G114	10149	121
159	C1BP	6438.5	-256	209	G16	10982	261	259	G116	10132	261
160	C1BM	6548.5	-256	210	G18	10965	121	260	G118	10115	121
161	C1BM	6658.5	-256	211	G20	10948	261	261	G120	10098	261
162	C1BM	6768.5	-256	212	G22	10931	121	262	G122	10081	121
163	C1CP	6878.5	-256	213	G24	10914	261	263	G124	10064	261
164	C1CP	6988.5	-256	214	G26	10897	121	264	G126	10047	121
165	C1CP	7098.5	-256	215	G28	10880	261	265	G128	10030	261
166	C1CM	7208.5	-256	216	G30	10863	121	266	G130	10013	121
167	C1CM	7318.5	-256	217	G32	10846	261	267	G132	9996	261
168	C1CM	7428.5	-256	218	G34	10829	121	268	G134	9979	121
169	PVDD	7538.5	-256	219	G36	10812	261	269	G136	9962	261
170	PVDD	7648.5	-256	220	G38	10795	121	270	G138	9945	121
171	PVDD	7758.5	-256	221	G40	10778	261	271	G140	9928	261
172	PVDD	7868.5	-256	222	G42	10761	121	272	G142	9911	121
173	PVDD	7978.5	-256	223	G44	10744	261	273	G144	9894	261
174	PVDD	8088.5	-256	224	G46	10727	121	274	G146	9877	121
175	PVDD	8198.5	-256	225	G48	10710	261	275	G148	9860	261
176	PVDD	8308.5	-256	226	G50	10693	121	276	G150	9843	121
177	C2P	8418.5	-256	227	G52	10676	261	277	G152	9826	261
178	C2P	8528.5	-256	228	G54	10659	121	278	G154	9809	121
179	C2M	8638.5	-256	229	G56	10642	261	279	G156	9792	261
180	C2M	8748.5	-256	230	G58	10625	121	280	G158	9775	121
181	VINT2	8858.5	-256	231	G60	10608	261	281	G160	9758	261
182	VINT2	8968.5	-256	232	G62	10591	121	282	G162	9741	121
183	VINT2	9078.5	-256	233	G64	10574	261	283	G164	9724	261
184	SHIELDING9	9188.5	-256	234	G66	10557	121	284	G166	9707	121
185	C3P	9298.5	-256	235	G68	10540	261	285	G168	9690	261
186	C3P	9408.5	-256	236	G70	10523	121	286	G170	9673	121
187	C3M	9518.5	-256	237	G72	10506	261	287	G172	9656	261
188	C3M	9628.5	-256	238	G74	10489	121	288	G174	9639	121
189	VGH	9738.5	-256	239	G76	10472	261	289	G176	9622	261
190	VGH	9848.5	-256	240	G78	10455	121	290	G178	9605	121
191	VGH	9958.5	-256	241	G80	10438	261	291	G180	9588	261
192	C4P	10068.5	-256	242	G82	10421	121	292	G182	9571	121
193	C4P	10178.5	-256	243	G84	10404	261	293	G184	9554	261
194	C4M	10288.5	-256	244	G86	10387	121	294	G186	9537	121
195	C4M	10398.5	-256	245	G88	10370	261	295	G188	9520	261
196	VGL	10508.5	-256	246	G90	10353	121	296	G190	9503	121
197	VGL	10618.5	-256	247	G92	10336	261	297	G192	9486	261
198	VGL	10728.5	-256	248	G94	10319	121	298	G194	9469	121
199	SHIELDING10	10838.5	-256	249	G96	10302	261	299	G196	9452	261
200	DUM	10948.5	-256	250	G98	10285	121	300	G198	9435	121

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
301	G200	9418	261	351	G300	8568	261	401	G400	7718	261
302	G202	9401	121	352	G302	8551	121	402	G402	7701	121
303	G204	9384	261	353	G304	8534	261	403	G404	7684	261
304	G206	9367	121	354	G306	8517	121	404	G406	7667	121
305	G208	9350	261	355	G308	8500	261	405	G408	7650	261
306	G210	9333	121	356	G310	8483	121	406	G410	7633	121
307	G212	9316	261	357	G312	8466	261	407	G412	7616	261
308	G214	9299	121	358	G314	8449	121	408	G414	7599	121
309	G216	9282	261	359	G316	8432	261	409	G416	7582	261
310	G218	9265	121	360	G318	8415	121	410	G418	7565	121
311	G220	9248	261	361	G320	8398	261	411	G420	7548	261
312	G222	9231	121	362	G322	8381	121	412	G422	7531	121
313	G224	9214	261	363	G324	8364	261	413	G424	7514	261
314	G226	9197	121	364	G326	8347	121	414	G426	7497	121
315	G228	9180	261	365	G328	8330	261	415	G428	7480	261
316	G230	9163	121	366	G330	8313	121	416	G430	7463	121
317	G232	9146	261	367	G332	8296	261	417	G432	7446	261
318	G234	9129	121	368	G334	8279	121	418	G434	7429	121
319	G236	9112	261	369	G336	8262	261	419	G436	7412	261
320	G238	9095	121	370	G338	8245	121	420	G438	7395	121
321	G240	9078	261	371	G340	8228	261	421	G440	7378	261
322	G242	9061	121	372	G342	8211	121	422	G442	7361	121
323	G244	9044	261	373	G344	8194	261	423	G444	7344	261
324	G246	9027	121	374	G346	8177	121	424	G446	7327	121
325	G248	9010	261	375	G348	8160	261	425	G448	7310	261
326	G250	8993	121	376	G350	8143	121	426	G450	7293	121
327	G252	8976	261	377	G352	8126	261	427	G452	7276	261
328	G254	8959	121	378	G354	8109	121	428	G454	7259	121
329	G256	8942	261	379	G356	8092	261	429	G456	7242	261
330	G258	8925	121	380	G358	8075	121	430	G458	7225	121
331	G260	8908	261	381	G360	8058	261	431	G460	7208	261
332	G262	8891	121	382	G362	8041	121	432	G462	7191	121
333	G264	8874	261	383	G364	8024	261	433	G464	7174	261
334	G266	8857	121	384	G366	8007	121	434	G466	7157	121
335	G268	8840	261	385	G368	7990	261	435	G468	7140	261
336	G270	8823	121	386	G370	7973	121	436	G470	7123	121
337	G272	8806	261	387	G372	7956	261	437	G472	7106	261
338	G274	8789	121	388	G374	7939	121	438	G474	7089	121
339	G276	8772	261	389	G376	7922	261	439	G476	7072	261
340	G278	8755	121	390	G378	7905	121	440	G478	7055	121
341	G280	8738	261	391	G380	7888	261	441	G480	7038	261
342	G282	8721	121	392	G382	7871	121	442	G482	7021	121
343	G284	8704	261	393	G384	7854	261	443	G484	7004	261
344	G286	8687	121	394	G386	7837	121	444	G486	6987	121
345	G288	8670	261	395	G388	7820	261	445	G488	6970	261
346	G290	8653	121	396	G390	7803	121	446	G490	6953	121
347	G292	8636	261	397	G392	7786	261	447	G492	6936	261
348	G294	8619	121	398	G394	7769	121	448	G494	6919	121
349	G296	8602	261	399	G396	7752	261	449	G496	6902	261
350	G298	8585	121	400	G398	7735	121	450	G498	6885	121

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
451	G500	6868	261	501	S23	5899	121	551	S73	5049	121
452	G502	6851	121	502	S24	5882	261	552	S74	5032	261
453	G504	6834	261	503	S25	5865	121	553	S75	5015	121
454	G506	6817	121	504	S26	5848	261	554	S76	4998	261
455	G508	6800	261	505	S27	5831	121	555	S77	4981	121
456	G510	6783	121	506	S28	5814	261	556	S78	4964	261
457	G512	6766	261	507	S29	5797	121	557	S79	4947	121
458	G514	6749	121	508	S30	5780	261	558	S80	4930	261
459	G516	6732	261	509	S31	5763	121	559	S81	4913	121
460	G518	6715	121	510	S32	5746	261	560	S82	4896	261
461	G520	6698	261	511	S33	5729	121	561	S83	4879	121
462	G522	6681	121	512	S34	5712	261	562	S84	4862	261
463	G524	6664	261	513	S35	5695	121	563	S85	4845	121
464	G526	6647	121	514	S36	5678	261	564	S86	4828	261
465	G528	6630	261	515	S37	5661	121	565	S87	4811	121
466	G530	6613	121	516	S38	5644	261	566	S88	4794	261
467	G532	6596	261	517	S39	5627	121	567	S89	4777	121
468	G534	6579	121	518	S40	5610	261	568	S90	4760	261
469	G536	6562	261	519	S41	5593	121	569	S91	4743	121
470	G538	6545	121	520	S42	5576	261	570	S92	4726	261
471	G540	6528	261	521	S43	5559	121	571	S93	4709	121
472	G542	6511	121	522	S44	5542	261	572	S94	4692	261
473	G544	6494	261	523	S45	5525	121	573	S95	4675	121
474	COM2_R	6443	261	524	S46	5508	261	574	S96	4658	261
475	COM2_R	6409	261	525	S47	5491	121	575	S97	4641	121
476	COM2_R	6375	261	526	S48	5474	261	576	S98	4624	261
477	COM2_R	6341	261	527	S49	5457	121	577	S99	4607	121
478	COM2_R	6307	261	528	S50	5440	261	578	S100	4590	261
479	S1	6273	121	529	S51	5423	121	579	S101	4573	121
480	S2	6256	261	530	S52	5406	261	580	S102	4556	261
481	S3	6239	121	531	S53	5389	121	581	S103	4539	121
482	S4	6222	261	532	S54	5372	261	582	S104	4522	261
483	S5	6205	121	533	S55	5355	121	583	S105	4505	121
484	S6	6188	261	534	S56	5338	261	584	S106	4488	261
485	S7	6171	121	535	S57	5321	121	585	S107	4471	121
486	S8	6154	261	536	S58	5304	261	586	S108	4454	261
487	S9	6137	121	537	S59	5287	121	587	S109	4437	121
488	S10	6120	261	538	S60	5270	261	588	S110	4420	261
489	S11	6103	121	539	S61	5253	121	589	S111	4403	121
490	S12	6086	261	540	S62	5236	261	590	S112	4386	261
491	S13	6069	121	541	S63	5219	121	591	S113	4369	121
492	S14	6052	261	542	S64	5202	261	592	S114	4352	261
493	S15	6035	121	543	S65	5185	121	593	S115	4335	121
494	S16	6018	261	544	S66	5168	261	594	S116	4318	261
495	S17	6001	121	545	S67	5151	121	595	S117	4301	121
496	S18	5984	261	546	S68	5134	261	596	S118	4284	261
497	S19	5967	121	547	S69	5117	121	597	S119	4267	121
498	S20	5950	261	548	S70	5100	261	598	S120	4250	261
499	S21	5933	121	549	S71	5083	121	599	S121	4233	121
500	S22	5916	261	550	S72	5066	261	600	S122	4216	261

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
601	S123	4199	121	651	S173	3349	121	701	S223	2499	121
602	S124	4182	261	652	S174	3332	261	702	S224	2482	261
603	S125	4165	121	653	S175	3315	121	703	S225	2465	121
604	S126	4148	261	654	S176	3298	261	704	S226	2448	261
605	S127	4131	121	655	S177	3281	121	705	S227	2431	121
606	S128	4114	261	656	S178	3264	261	706	S228	2414	261
607	S129	4097	121	657	S179	3247	121	707	S229	2397	121
608	S130	4080	261	658	S180	3230	261	708	S230	2380	261
609	S131	4063	121	659	S181	3213	121	709	S231	2363	121
610	S132	4046	261	660	S182	3196	261	710	S232	2346	261
611	S133	4029	121	661	S183	3179	121	711	S233	2329	121
612	S134	4012	261	662	S184	3162	261	712	S234	2312	261
613	S135	3995	121	663	S185	3145	121	713	S235	2295	121
614	S136	3978	261	664	S186	3128	261	714	S236	2278	261
615	S137	3961	121	665	S187	3111	121	715	S237	2261	121
616	S138	3944	261	666	S188	3094	261	716	S238	2244	261
617	S139	3927	121	667	S189	3077	121	717	S239	2227	121
618	S140	3910	261	668	S190	3060	261	718	S240	2210	261
619	S141	3893	121	669	S191	3043	121	719	S241	2193	121
620	S142	3876	261	670	S192	3026	261	720	S242	2176	261
621	S143	3859	121	671	S193	3009	121	721	S243	2159	121
622	S144	3842	261	672	S194	2992	261	722	S244	2142	261
623	S145	3825	121	673	S195	2975	121	723	S245	2125	121
624	S146	3808	261	674	S196	2958	261	724	S246	2108	261
625	S147	3791	121	675	S197	2941	121	725	S247	2091	121
626	S148	3774	261	676	S198	2924	261	726	S248	2074	261
627	S149	3757	121	677	S199	2907	121	727	S249	2057	121
628	S150	3740	261	678	S200	2890	261	728	S250	2040	261
629	S151	3723	121	679	S201	2873	121	729	S251	2023	121
630	S152	3706	261	680	S202	2856	261	730	S252	2006	261
631	S153	3689	121	681	S203	2839	121	731	S253	1989	121
632	S154	3672	261	682	S204	2822	261	732	S254	1972	261
633	S155	3655	121	683	S205	2805	121	733	S255	1955	121
634	S156	3638	261	684	S206	2788	261	734	S256	1938	261
635	S157	3621	121	685	S207	2771	121	735	S257	1921	121
636	S158	3604	261	686	S208	2754	261	736	S258	1904	261
637	S159	3587	121	687	S209	2737	121	737	S259	1887	121
638	S160	3570	261	688	S210	2720	261	738	S260	1870	261
639	S161	3553	121	689	S211	2703	121	739	S261	1853	121
640	S162	3536	261	690	S212	2686	261	740	S262	1836	261
641	S163	3519	121	691	S213	2669	121	741	S263	1819	121
642	S164	3502	261	692	S214	2652	261	742	S264	1802	261
643	S165	3485	121	693	S215	2635	121	743	S265	1785	121
644	S166	3468	261	694	S216	2618	261	744	S266	1768	261
645	S167	3451	121	695	S217	2601	121	745	S267	1751	121
646	S168	3434	261	696	S218	2584	261	746	S268	1734	261
647	S169	3417	121	697	S219	2567	121	747	S269	1717	121
648	S170	3400	261	698	S220	2550	261	748	S270	1700	261
649	S171	3383	121	699	S221	2533	121	749	S271	1683	121
650	S172	3366	261	700	S222	2516	261	750	S272	1666	261

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
751	S273	1649	121	801	S323	799	121	851	S365	-238	261
752	S274	1632	261	802	S324	782	261	852	S366	-255	121
753	S275	1615	121	803	S325	765	121	853	S367	-272	261
754	S276	1598	261	804	S326	748	261	854	S368	-289	121
755	S277	1581	121	805	S327	731	121	855	S369	-306	261
756	S278	1564	261	806	S328	714	261	856	S370	-323	121
757	S279	1547	121	807	S329	697	121	857	S371	-340	261
758	S280	1530	261	808	S330	680	261	858	S372	-357	121
759	S281	1513	121	809	S331	663	121	859	S373	-374	261
760	S282	1496	261	810	S332	646	261	860	S374	-391	121
761	S283	1479	121	811	S333	629	121	861	S375	-408	261
762	S284	1462	261	812	S334	612	261	862	S376	-425	121
763	S285	1445	121	813	S335	595	121	863	S377	-442	261
764	S286	1428	261	814	S336	578	261	864	S378	-459	121
765	S287	1411	121	815	S337	561	121	865	S379	-476	261
766	S288	1394	261	816	S338	544	261	866	S380	-493	121
767	S289	1377	121	817	S339	527	121	867	S381	-510	261
768	S290	1360	261	818	S340	510	261	868	S382	-527	121
769	S291	1343	121	819	S341	493	121	869	S383	-544	261
770	S292	1326	261	820	S342	476	261	870	S384	-561	121
771	S293	1309	121	821	S343	459	121	871	S385	-578	261
772	S294	1292	261	822	S344	442	261	872	S386	-595	121
773	S295	1275	121	823	S345	425	121	873	S387	-612	261
774	S296	1258	261	824	S346	408	261	874	S388	-629	121
775	S297	1241	121	825	S347	391	121	875	S389	-646	261
776	S298	1224	261	826	S348	374	261	876	S390	-663	121
777	S299	1207	121	827	S349	357	121	877	S391	-680	261
778	S300	1190	261	828	S350	340	261	878	S392	-697	121
779	S301	1173	121	829	S351	323	121	879	S393	-714	261
780	S302	1156	261	830	S352	306	261	880	S394	-731	121
781	S303	1139	121	831	S353	289	121	881	S395	-748	261
782	S304	1122	261	832	S354	272	261	882	S396	-765	121
783	S305	1105	121	833	S355	255	121	883	S397	-782	261
784	S306	1088	261	834	S356	238	261	884	S398	-799	121
785	S307	1071	121	835	S357	221	121	885	S399	-816	261
786	S308	1054	261	836	S358	204	261	886	S400	-833	121
787	S309	1037	121	837	S359	187	121	887	S401	-850	261
788	S310	1020	261	838	S360	170	261	888	S402	-867	121
789	S311	1003	121	839	DCMP	119	261	889	S403	-884	261
790	S312	986	261	840	DCMP	85	261	890	S404	-901	121
791	S313	969	121	841	DCMP	51	261	891	S405	-918	261
792	S314	952	261	842	DCMP	17	261	892	S406	-935	121
793	S315	935	121	843	DCMP	-17	261	893	S407	-952	261
794	S316	918	261	844	DCMP	-51	261	894	S408	-969	121
795	S317	901	121	845	DCMP	-85	261	895	S409	-986	261
796	S318	884	261	846	DCMP	-119	261	896	S410	-1003	121
797	S319	867	121	847	S361	-170	261	897	S411	-1020	261
798	S320	850	261	848	S362	-187	121	898	S412	-1037	121
799	S321	833	121	849	S363	-204	261	899	S413	-1054	261
800	S322	816	261	850	S364	-221	121	900	S414	-1071	121

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
901	S415	-1088	261	951	S465	-1938	261	1001	S515	-2788	261
902	S416	-1105	121	952	S466	-1955	121	1002	S516	-2805	121
903	S417	-1122	261	953	S467	-1972	261	1003	S517	-2822	261
904	S418	-1139	121	954	S468	-1989	121	1004	S518	-2839	121
905	S419	-1156	261	955	S469	-2006	261	1005	S519	-2856	261
906	S420	-1173	121	956	S470	-2023	121	1006	S520	-2873	121
907	S421	-1190	261	957	S471	-2040	261	1007	S521	-2890	261
908	S422	-1207	121	958	S472	-2057	121	1008	S522	-2907	121
909	S423	-1224	261	959	S473	-2074	261	1009	S523	-2924	261
910	S424	-1241	121	960	S474	-2091	121	1010	S524	-2941	121
911	S425	-1258	261	961	S475	-2108	261	1011	S525	-2958	261
912	S426	-1275	121	962	S476	-2125	121	1012	S526	-2975	121
913	S427	-1292	261	963	S477	-2142	261	1013	S527	-2992	261
914	S428	-1309	121	964	S478	-2159	121	1014	S528	-3009	121
915	S429	-1326	261	965	S479	-2176	261	1015	S529	-3026	261
916	S430	-1343	121	966	S480	-2193	121	1016	S530	-3043	121
917	S431	-1360	261	967	S481	-2210	261	1017	S531	-3060	261
918	S432	-1377	121	968	S482	-2227	121	1018	S532	-3077	121
919	S433	-1394	261	969	S483	-2244	261	1019	S533	-3094	261
920	S434	-1411	121	970	S484	-2261	121	1020	S534	-3111	121
921	S435	-1428	261	971	S485	-2278	261	1021	S535	-3128	261
922	S436	-1445	121	972	S486	-2295	121	1022	S536	-3145	121
923	S437	-1462	261	973	S487	-2312	261	1023	S537	-3162	261
924	S438	-1479	121	974	S488	-2329	121	1024	S538	-3179	121
925	S439	-1496	261	975	S489	-2346	261	1025	S539	-3196	261
926	S440	-1513	121	976	S490	-2363	121	1026	S540	-3213	121
927	S441	-1530	261	977	S491	-2380	261	1027	S541	-3230	261
928	S442	-1547	121	978	S492	-2397	121	1028	S542	-3247	121
929	S443	-1564	261	979	S493	-2414	261	1029	S543	-3264	261
930	S444	-1581	121	980	S494	-2431	121	1030	S544	-3281	121
931	S445	-1598	261	981	S495	-2448	261	1031	S545	-3298	261
932	S446	-1615	121	982	S496	-2465	121	1032	S546	-3315	121
933	S447	-1632	261	983	S497	-2482	261	1033	S547	-3332	261
934	S448	-1649	121	984	S498	-2499	121	1034	S548	-3349	121
935	S449	-1666	261	985	S499	-2516	261	1035	S549	-3366	261
936	S450	-1683	121	986	S500	-2533	121	1036	S550	-3383	121
937	S451	-1700	261	987	S501	-2550	261	1037	S551	-3400	261
938	S452	-1717	121	988	S502	-2567	121	1038	S552	-3417	121
939	S453	-1734	261	989	S503	-2584	261	1039	S553	-3434	261
940	S454	-1751	121	990	S504	-2601	121	1040	S554	-3451	121
941	S455	-1768	261	991	S505	-2618	261	1041	S555	-3468	261
942	S456	-1785	121	992	S506	-2635	121	1042	S556	-3485	121
943	S457	-1802	261	993	S507	-2652	261	1043	S557	-3502	261
944	S458	-1819	121	994	S508	-2669	121	1044	S558	-3519	121
945	S459	-1836	261	995	S509	-2686	261	1045	S559	-3536	261
946	S460	-1853	121	996	S510	-2703	121	1046	S560	-3553	121
947	S461	-1870	261	997	S511	-2720	261	1047	S561	-3570	261
948	S462	-1887	121	998	S512	-2737	121	1048	S562	-3587	121
949	S463	-1904	261	999	S513	-2754	261	1049	S563	-3604	261
950	S464	-1921	121	1000	S514	-2771	121	1050	S564	-3621	121

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1051	S565	-3638	261	1101	S615	-4488	261	1151	S665	-5338	261
1052	S566	-3655	121	1102	S616	-4505	121	1152	S666	-5355	121
1053	S567	-3672	261	1103	S617	-4522	261	1153	S667	-5372	261
1054	S568	-3689	121	1104	S618	-4539	121	1154	S668	-5389	121
1055	S569	-3706	261	1105	S619	-4556	261	1155	S669	-5406	261
1056	S570	-3723	121	1106	S620	-4573	121	1156	S670	-5423	121
1057	S571	-3740	261	1107	S621	-4590	261	1157	S671	-5440	261
1058	S572	-3757	121	1108	S622	-4607	121	1158	S672	-5457	121
1059	S573	-3774	261	1109	S623	-4624	261	1159	S673	-5474	261
1060	S574	-3791	121	1110	S624	-4641	121	1160	S674	-5491	121
1061	S575	-3808	261	1111	S625	-4658	261	1161	S675	-5508	261
1062	S576	-3825	121	1112	S626	-4675	121	1162	S676	-5525	121
1063	S577	-3842	261	1113	S627	-4692	261	1163	S677	-5542	261
1064	S578	-3859	121	1114	S628	-4709	121	1164	S678	-5559	121
1065	S579	-3876	261	1115	S629	-4726	261	1165	S679	-5576	261
1066	S580	-3893	121	1116	S630	-4743	121	1166	S680	-5593	121
1067	S581	-3910	261	1117	S631	-4760	261	1167	S681	-5610	261
1068	S582	-3927	121	1118	S632	-4777	121	1168	S682	-5627	121
1069	S583	-3944	261	1119	S633	-4794	261	1169	S683	-5644	261
1070	S584	-3961	121	1120	S634	-4811	121	1170	S684	-5661	121
1071	S585	-3978	261	1121	S635	-4828	261	1171	S685	-5678	261
1072	S586	-3995	121	1122	S636	-4845	121	1172	S686	-5695	121
1073	S587	-4012	261	1123	S637	-4862	261	1173	S687	-5712	261
1074	S588	-4029	121	1124	S638	-4879	121	1174	S688	-5729	121
1075	S589	-4046	261	1125	S639	-4896	261	1175	S689	-5746	261
1076	S590	-4063	121	1126	S640	-4913	121	1176	S690	-5763	121
1077	S591	-4080	261	1127	S641	-4930	261	1177	S691	-5780	261
1078	S592	-4097	121	1128	S642	-4947	121	1178	S692	-5797	121
1079	S593	-4114	261	1129	S643	-4964	261	1179	S693	-5814	261
1080	S594	-4131	121	1130	S644	-4981	121	1180	S694	-5831	121
1081	S595	-4148	261	1131	S645	-4998	261	1181	S695	-5848	261
1082	S596	-4165	121	1132	S646	-5015	121	1182	S696	-5865	121
1083	S597	-4182	261	1133	S647	-5032	261	1183	S697	-5882	261
1084	S598	-4199	121	1134	S648	-5049	121	1184	S698	-5899	121
1085	S599	-4216	261	1135	S649	-5066	261	1185	S699	-5916	261
1086	S600	-4233	121	1136	S650	-5083	121	1186	S700	-5933	121
1087	S601	-4250	261	1137	S651	-5100	261	1187	S701	-5950	261
1088	S602	-4267	121	1138	S652	-5117	121	1188	S702	-5967	121
1089	S603	-4284	261	1139	S653	-5134	261	1189	S703	-5984	261
1090	S604	-4301	121	1140	S654	-5151	121	1190	S704	-6001	121
1091	S605	-4318	261	1141	S655	-5168	261	1191	S705	-6018	261
1092	S606	-4335	121	1142	S656	-5185	121	1192	S706	-6035	121
1093	S607	-4352	261	1143	S657	-5202	261	1193	S707	-6052	261
1094	S608	-4369	121	1144	S658	-5219	121	1194	S708	-6069	121
1095	S609	-4386	261	1145	S659	-5236	261	1195	S709	-6086	261
1096	S610	-4403	121	1146	S660	-5253	121	1196	S710	-6103	121
1097	S611	-4420	261	1147	S661	-5270	261	1197	S711	-6120	261
1098	S612	-4437	121	1148	S662	-5287	121	1198	S712	-6137	121
1099	S613	-4454	261	1149	S663	-5304	261	1199	S713	-6154	261
1100	S614	-4471	121	1150	S664	-5321	121	1200	S714	-6171	121

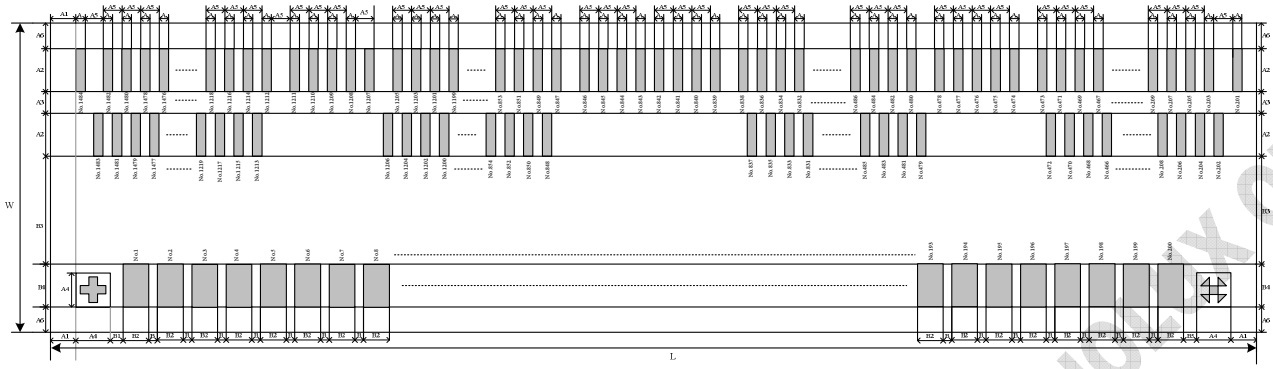
Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1201	S715	-6188	261	1251	G465	-7157	121	1301	G365	-8007	121
1202	S716	-6205	121	1252	G463	-7174	261	1302	G363	-8024	261
1203	S717	-6222	261	1253	G461	-7191	121	1303	G361	-8041	121
1204	S718	-6239	121	1254	G459	-7208	261	1304	G359	-8058	261
1205	S719	-6256	261	1255	G457	-7225	121	1305	G357	-8075	121
1206	S720	-6273	121	1256	G455	-7242	261	1306	G355	-8092	261
1207	COM1_R	-6307	261	1257	G453	-7259	121	1307	G353	-8109	121
1208	COM1_R	-6341	261	1258	G451	-7276	261	1308	G351	-8126	261
1209	COM1_R	-6375	261	1259	G449	-7293	121	1309	G349	-8143	121
1210	COM1_R	-6409	261	1260	G447	-7310	261	1310	G347	-8160	261
1211	COM1_R	-6443	261	1261	G445	-7327	121	1311	G345	-8177	121
1212	G543	-6494	261	1262	G443	-7344	261	1312	G343	-8194	261
1213	G541	-6511	121	1263	G441	-7361	121	1313	G341	-8211	121
1214	G539	-6528	261	1264	G439	-7378	261	1314	G339	-8228	261
1215	G537	-6545	121	1265	G437	-7395	121	1315	G337	-8245	121
1216	G535	-6562	261	1266	G435	-7412	261	1316	G335	-8262	261
1217	G533	-6579	121	1267	G433	-7429	121	1317	G333	-8279	121
1218	G531	-6596	261	1268	G431	-7446	261	1318	G331	-8296	261
1219	G529	-6613	121	1269	G429	-7463	121	1319	G329	-8313	121
1220	G527	-6630	261	1270	G427	-7480	261	1320	G327	-8330	261
1221	G525	-6647	121	1271	G425	-7497	121	1321	G325	-8347	121
1222	G523	-6664	261	1272	G423	-7514	261	1322	G323	-8364	261
1223	G521	-6681	121	1273	G421	-7531	121	1323	G321	-8381	121
1224	G519	-6698	261	1274	G419	-7548	261	1324	G319	-8398	261
1225	G517	-6715	121	1275	G417	-7565	121	1325	G317	-8415	121
1226	G515	-6732	261	1276	G415	-7582	261	1326	G315	-8432	261
1227	G513	-6749	121	1277	G413	-7599	121	1327	G313	-8449	121
1228	G511	-6766	261	1278	G411	-7616	261	1328	G311	-8466	261
1229	G509	-6783	121	1279	G409	-7633	121	1329	G309	-8483	121
1230	G507	-6800	261	1280	G407	-7650	261	1330	G307	-8500	261
1231	G505	-6817	121	1281	G405	-7667	121	1331	G305	-8517	121
1232	G503	-6834	261	1282	G403	-7684	261	1332	G303	-8534	261
1233	G501	-6851	121	1283	G401	-7701	121	1333	G301	-8551	121
1234	G499	-6868	261	1284	G399	-7718	261	1334	G299	-8568	261
1235	G497	-6885	121	1285	G397	-7735	121	1335	G297	-8585	121
1236	G495	-6902	261	1286	G395	-7752	261	1336	G295	-8602	261
1237	G493	-6919	121	1287	G393	-7769	121	1337	G293	-8619	121
1238	G491	-6936	261	1288	G391	-7786	261	1338	G291	-8636	261
1239	G489	-6953	121	1289	G389	-7803	121	1339	G289	-8653	121
1240	G487	-6970	261	1290	G387	-7820	261	1340	G287	-8670	261
1241	G485	-6987	121	1291	G385	-7837	121	1341	G285	-8687	121
1242	G483	-7004	261	1292	G383	-7854	261	1342	G283	-8704	261
1243	G481	-7021	121	1293	G381	-7871	121	1343	G281	-8721	121
1244	G479	-7038	261	1294	G379	-7888	261	1344	G279	-8738	261
1245	G477	-7055	121	1295	G377	-7905	121	1345	G277	-8755	121
1246	G475	-7072	261	1296	G375	-7922	261	1346	G275	-8772	261
1247	G473	-7089	121	1297	G373	-7939	121	1347	G273	-8789	121
1248	G471	-7106	261	1298	G371	-7956	261	1348	G271	-8806	261
1249	G469	-7123	121	1299	G369	-7973	121	1349	G269	-8823	121
1250	G467	-7140	261	1300	G367	-7990	261	1350	G267	-8840	261

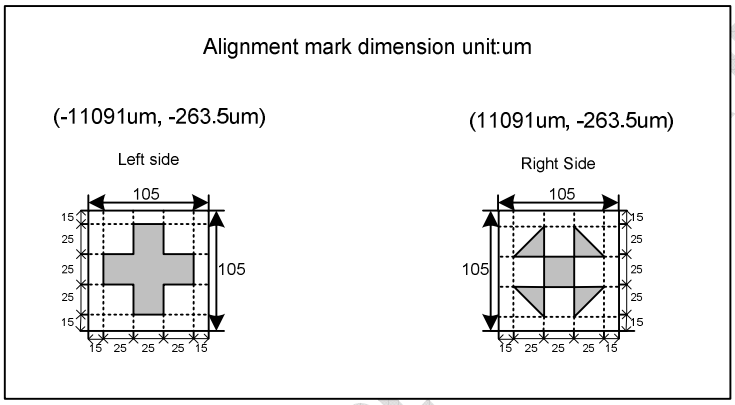
Pad No.	Designation	CX	CY
1351	G265	-8857	121
1352	G263	-8874	261
1353	G261	-8891	121
1354	G259	-8908	261
1355	G257	-8925	121
1356	G255	-8942	261
1357	G253	-8959	121
1358	G251	-8976	261
1359	G249	-8993	121
1360	G247	-9010	261
1361	G245	-9027	121
1362	G243	-9044	261
1363	G241	-9061	121
1364	G239	-9078	261
1365	G237	-9095	121
1366	G235	-9112	261
1367	G233	-9129	121
1368	G231	-9146	261
1369	G229	-9163	121
1370	G227	-9180	261
1371	G225	-9197	121
1372	G223	-9214	261
1373	G221	-9231	121
1374	G219	-9248	261
1375	G217	-9265	121
1376	G215	-9282	261
1377	G213	-9299	121
1378	G211	-9316	261
1379	G209	-9333	121
1380	G207	-9350	261
1381	G205	-9367	121
1382	G203	-9384	261
1383	G201	-9401	121
1384	G199	-9418	261
1385	G197	-9435	121
1386	G195	-9452	261
1387	G193	-9469	121
1388	G191	-9486	261
1389	G189	-9503	121
1390	G187	-9520	261
1391	G185	-9537	121
1392	G183	-9554	261
1393	G181	-9571	121
1394	G179	-9588	261
1395	G177	-9605	121
1396	G175	-9622	261
1397	G173	-9639	121
1398	G171	-9656	261
1399	G169	-9673	121
1400	G167	-9690	261

Pad No.	Designation	CX	CY
1401	G165	-9707	121
1402	G163	-9724	261
1403	G161	-9741	121
1404	G159	-9758	261
1405	G157	-9775	121
1406	G155	-9792	261
1407	G153	-9809	121
1408	G151	-9826	261
1409	G149	-9843	121
1410	G147	-9860	261
1411	G145	-9877	121
1412	G143	-9894	261
1413	G141	-9911	121
1414	G139	-9928	261
1415	G137	-9945	121
1416	G135	-9962	261
1417	G133	-9979	121
1418	G131	-9996	261
1419	G129	-10013	121
1420	G127	-10030	261
1421	G125	-10047	121
1422	G123	-10064	261
1423	G121	-10081	121
1424	G119	-10098	261
1425	G117	-10115	121
1426	G115	-10132	261
1427	G113	-10149	121
1428	G111	-10166	261
1429	G109	-10183	121
1430	G107	-10200	261
1431	G105	-10217	121
1432	G103	-10234	261
1433	G101	-10251	121
1434	G99	-10268	261
1435	G97	-10285	121
1436	G95	-10302	261
1437	G93	-10319	121
1438	G91	-10336	261
1439	G89	-10353	121
1440	G87	-10370	261
1441	G85	-10387	121
1442	G83	-10404	261
1443	G81	-10421	121
1444	G79	-10438	261
1445	G77	-10455	121
1446	G75	-10472	261
1447	G73	-10489	121
1448	G71	-10506	261
1449	G69	-10523	121
1450	G67	-10540	261

Pad No.	Designation	CX	CY
1451	G65	-10557	121
1452	G63	-10574	261
1453	G61	-10591	121
1454	G59	-10608	261
1455	G57	-10625	121
1456	G55	-10642	261
1457	G53	-10659	121
1458	G51	-10676	261
1459	G49	-10693	121
1460	G47	-10710	261
1461	G45	-10727	121
1462	G43	-10744	261
1463	G41	-10761	121
1464	G39	-10778	261
1465	G37	-10795	121
1466	G35	-10812	261
1467	G33	-10829	121
1468	G31	-10846	261
1469	G29	-10863	121
1470	G27	-10880	261
1471	G25	-10897	121
1472	G23	-10914	261
1473	G21	-10931	121
1474	G19	-10948	261
1475	G17	-10965	121
1476	G15	-10982	261
1477	G13	-10999	121
1478	G11	-11016	261
1479	G9	-11033	121
1480	G7	-11050	261
1481	G5	-11067	121
1482	G3	-11084	261
1483	G1	-11101	121
1484	DUM	-11135	261

16. Bump Mask Information





(1)120umx80um: No.1~200

(2)110umx17um: No201~1484

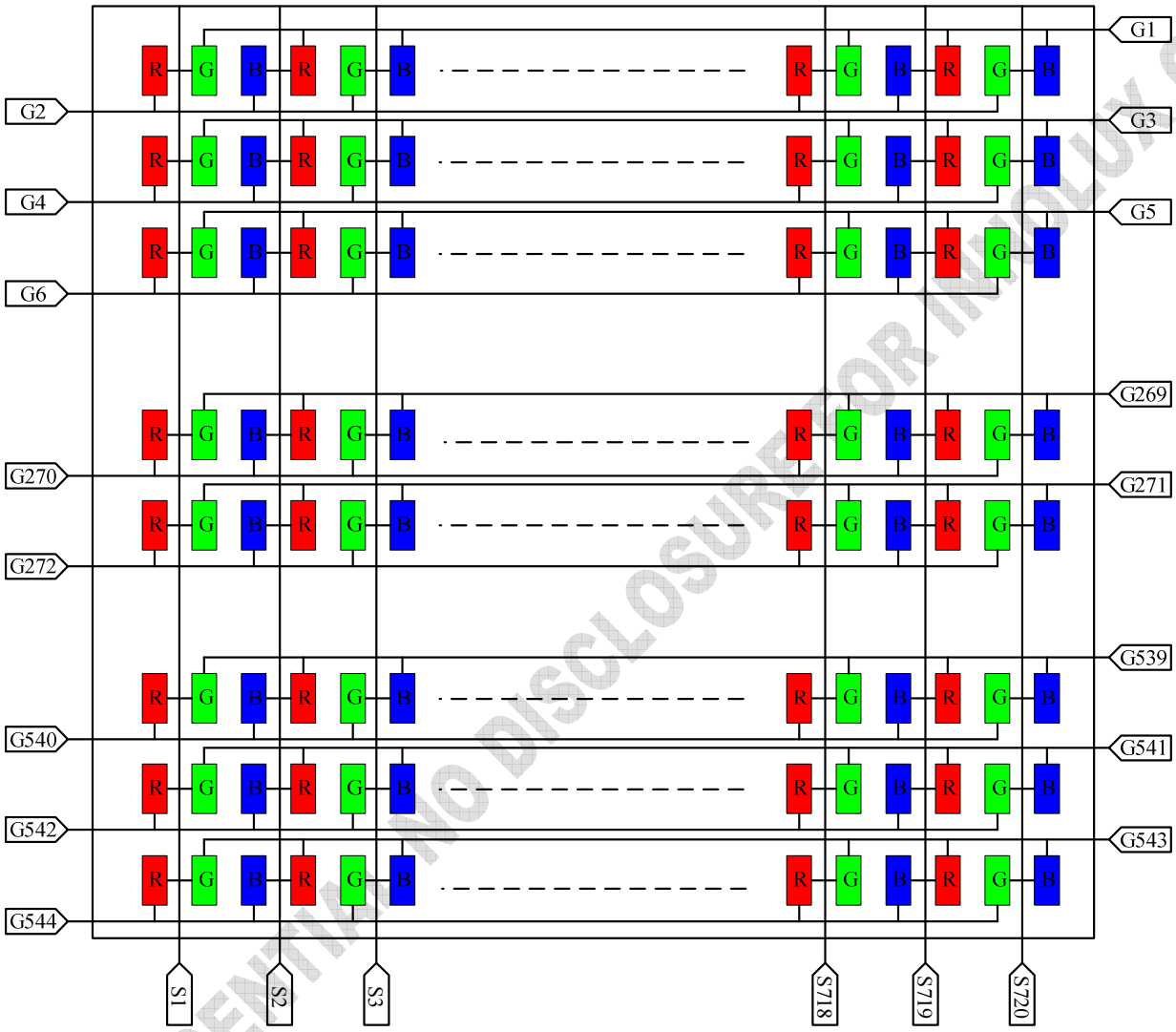
(3)105umx105um: Alignment mark

Symbol	Dimensions(um)	Symbol	Dimensions (um)	Symbol	Dimensions (um)
A	17	B	30	W	732(Max)
A1	59	B1	57	L	22405(Max)
A2	110	B2	80		
A3	30	B3	262		
A4	105	B4	120		
A5	34	B5	50		
A6	50				

*Remark: Chip dimension include scribe line

17. Color Filter Arrangement

The stripe color filter arrangement is shown below:



18. Revision History

Version No.	Date	Page	Description
0.00	2009/01/22	All	New Create
0.01	2009/01/22	P59	Correct the chip length from 22405um to 22387um
0.02	2009/02/05	P4 P35 P43 P60	Modify Application circuit Modify Charge-pump Circuit Connection & Component list Modify Electronic Characteristic – VCOML condition Modify A1 and W dimension size
0.03	2009/02/17	P43	Add VINT1 in DC characteristics
0.04	2009/04/01	P38 P44 P59	Modify Gamma voltages Add Tcwl and Tcwh specification Add color filter arrangement
0.05	2009/05/27	P9 P56	Modify Pin TCSW0 default setting H → L Modify Bump Mask Information
0.06	2009/06/11	P56	Modify Alignment Mark Information
0.07	2009/06/25	P4 P6 P13 P16 P21 P22 P25 P29 P30	Modify Charge-pump Circuit Modify the misspell words
0.08	2010/06/02	P43	Modify the Max. Value of VSD front porch
		P12 P18 P19	Modify VCOMH/VCOML default Value